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Two-Dimensional Electronic Materials and Devices: Opportunities and Challenges

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Two-Dimensional Electronic Materials and Devices: Opportunities and Challenges

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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September 2017

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ABSTRACT

Two-Dimensional Electronic Materials and Devices: Opportunities and Challenges

by

Jiahao Kang

The unprecedented growth of the *Internet of Things* (*IoT*) and the *4th Industrial Revolution* (*Industry 4.0*) not only demands dimensional scaling of device technologies but also new types of applications beyond today's electronics. Two-dimensional (2D) materials, a group of layered crystals (such as graphene and MoS_2) with unique properties, have emerged as promising candidates for *IoT* and *Industry 4.0* since they can, not only extend the scaling with unprecedented performance and energy efficiency but also exhibit high potential for novel electronic devices. However, such nanomaterials suffer from significant challenges in process integration, especially in the modules that involves the formation of interfaces between 2D materials and conventional bulk materials. Thus, realizing high-performance energy-efficient 2D electronic devices has been challenging. This dissertation focuses on understanding the fundamental issues in such 2D materials (such as contacts, interfaces and doping) and in identifying applications uniquely enabled by these materials.

First, a comprehensive treatment of metal contacts to 2D semiconductors, which has been a huge hurdle for 2D electronic technologies, will be presented. As a pioneering study, new interface physics originating from the unique dimensionality and surface properties have been revealed **[1]**. Solutions to minimize contact resistance are described though

techniques of interface hybridization **[2]** and seamless contacts **[3], [4]**. These techniques transform 2D semiconductors from solely scientifically-interesting materials into high-performance field-effect transistor (FET) technologies, such as MoS_2 FETs with record-low contact resistances **[5], [6]** and WSe_2 FETs with record-high drive current and mobility **[7]**.

Beyond metal interfaces, dielectric interface is crucial for preserving the carrier mobility in 2D channels, for which a solution enabled by buffer layers has been proposed **[8]**. On the other hand, the vertical van der Waals interfaces between 2D and 3D semiconductors, which retain the advantages of pristine ultra-thin 2D films as well as maximized tunneling area/field, have been studied and exploited into a novel beyond-silicon transistor technology – the first 2D channel tunnel FET (TFET) **[9]**, which beat the fundamental limitation in the switching behavior of transistors. Recent results from the engineering of such 2D-3D semiconductor interfaces by surface reduction/passivation are described, showing a significant boost of drive current.

While conventional diffusion/ion implantation methods are infeasible for 2D materials, two efficient doping techniques that are specific for 2D materials – surface doping **[10], [11]** and intercalation doping **[12]** are presented. The theoretical study of surface doping using ab-initio methods helped develop a novel doping scheme that uniquely exploits the Lewis-base like pedigree of 2D semiconductors without disturbing the structural integrity of the 2D atomic layer configuration **[13]**, as well as a novel electrocatalyst based on MoS_2 that achieved record high hydrogen evolution reaction (HER) performance **[14]**. On the other hand, intercalation doping has been employed to demonstrate graphene based transparent electrodes with the best combination of transmittance and sheet resistance **[12]**, and also the first graphene interconnects with excellent performance, reliability and energy-efficiency **[15], [16]**.

Moreover, by uniquely exploiting the high kinetic inductance and conductivity of intercalation doped graphene, a fundamentally different on-chip inductor has been demonstrated **[17], [18]**, with both small form-factors and high inductance values, that were once thought unachievable in tandem. This 2D technique provides an attractive solution to the longstanding scaling problem of analog/radio-frequency electronics and opens up an unconventional pathway for the development of future ultra-compact wireless communication systems.

Finally, a novel dissipative quantum transport methodology based on Büttiker probes with band-to-band tunneling capability is developed for 2D FETs **[19]**. Subsequently, gate-induced-drain-leakage (GIDL), one of the main leakage mechanisms in FETs especially access transistors, is evaluated for the first time for 2D FETs. The results establish the advantages of certain 2D semiconductors in greatly reducing GIDL and thereby support use of such materials in future memory technologies.

The dissertation concludes with a vision for how a smart life can be realized in the future by harnessing the capabilities of various 2D technologies in the era of *IoT* and *Industry 4.0*.

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I. Introduction

A. Two-Dimensional Electronic Materials

The emerging paradigm of *Internet of Things* (IoT), which promises unprecedented connectivity between people and up to 50 billion "things" by 2020 **[20], [21]** with a potential economic impact of US$2.7 trillion to $6.2 trillion per year by 2025 **[20], [22]**, will require tremendous amount of electronic devices with high scalability as well as new forms of electronics such as flexible and transparent electronics.

As silicon technology approaches its limits in scaling, alternative material systems to silicon have been pursued for future electronics. Recent advances in the realization of electronic devices **[7], [23]–[25]**, optical characterization **[26], [27]** and material preparation **[28]** have resulted in the revival of scientific interest in a material family with a wide range of electrical properties – the two-dimensional (2D) electronic materials (**Figure 1**), such as graphene, transition metal dichalcogenides (TMDs), phosphorene **[29]** and silicene **[30]**, etc.

With extremely small thicknesses (few Å), uniform band gap over a large area, and pristine interfaces without out-of-plane dangling bonds, they have the potential to allow efficient electrostatics **[24]**, reduction of short channel effects for nanoscale transistors **[31]**, fewer traps on a semiconductor-dielectric interface, and a high degree of vertical scaling. They also show many other attractive features exquisite sensing capabilities **[32]**, high breakdown voltages **[33]**, as well as tunable optical properties **[26], [27], [34]–[36]**, high degree of mechanical flexibility **[37]** and the possibility of engineering new materials through the realization of van der Waals heterostructures **[38]**. The 2D TMD materials are also attractive for display electronics **[39]** due to their inherent flexibility, transparency, and dangling-bond-free interface that make them easy to integrate with various substrates.

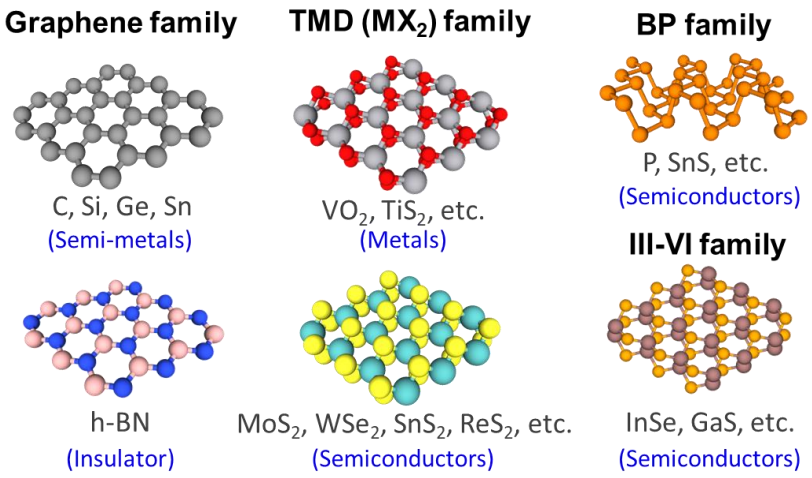


Figure 1: Representative families of 2D materials.

B. Opportunities of 2D Electronics

1. Technology Scaling – Transistors

The atomic scale thicknesses of 2D semiconductors offer high scalability to field-effect transistors (FETs) using them as channel materials, which is the primary motivation for researchers to explore them for FET application in sub-10 nanometer nodes **[23], [31]**. Although conventional bulk semiconductors such as silicon and germanium can also be made very thin, 2D semiconductors own extra advantages, specifically, atomically-smooth and dangling bond-free surface, and uniform and fixed (with the number of layers) thickness, as schematically shown in the next chapter. These advantages intrinsically suppresses possible trap generation, carrier scattering, and thickness (and hence band gap) variation, guaranteeing a robust device performance. In fact, by comparing the carrier mobilities in MoS_2 **[5], [40]**, the most widely studied 2D semiconductor, and in the mainstream Si **[41]** during thickness scaling, it is found that mobility degradation rate with

decreasing thickness in MoS_2 is much slower w.r.t. Si, leading to higher mobility at the extremely scaled thickness. With continuous improvement in material quality, and proper gate dielectric engineering, the mobilities in MoS_2 and other 2D materials can be further improved, as recently demonstrated by Liu et al. with the mobility in monolayer MoS_2 boosted to 44 cm^2/Vs **[42]**. Note that FET channel thickness scaling is imposed by gate length scaling as reflected by a general scaling formula **[43], [44]**:

$$L_{g,min} \geq \alpha \sqrt{t_{ch} t_{ox} \varepsilon_{ch} / \varepsilon_{ox}} \quad (1)$$

where $L_{g,min}$ is the minimum gate length in order to maintain good device electrostatics, α is a constant determined by gate geometry, t_{ch} (t_{ox}) is the channel (gate oxide) thickness, and ε_{ch} (ε_{ox}) is the dielectric constant of channel (gate oxide). The ultra-small t_{ch} (**Figure 2**) of 2D semiconductors enable ultra-small $L_{g,min}$ of 2D FETs.

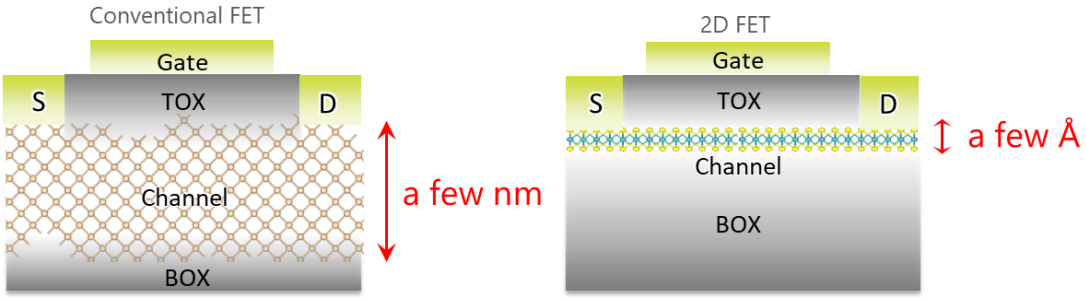


Figure 2: Channel thickness of conventional bulk FET and 2D FET.

Moreover, FET-based biosensors with 2D TMD semiconductor as the channel material have recently been demonstrated **[32]** to be highly advantageous over all other nanomaterial-based (including graphene) FET biosensors, due to their atomically layered and planar nature, nonzero band gaps, and pristine surfaces.

2. Technology Scaling – Steep Transistors

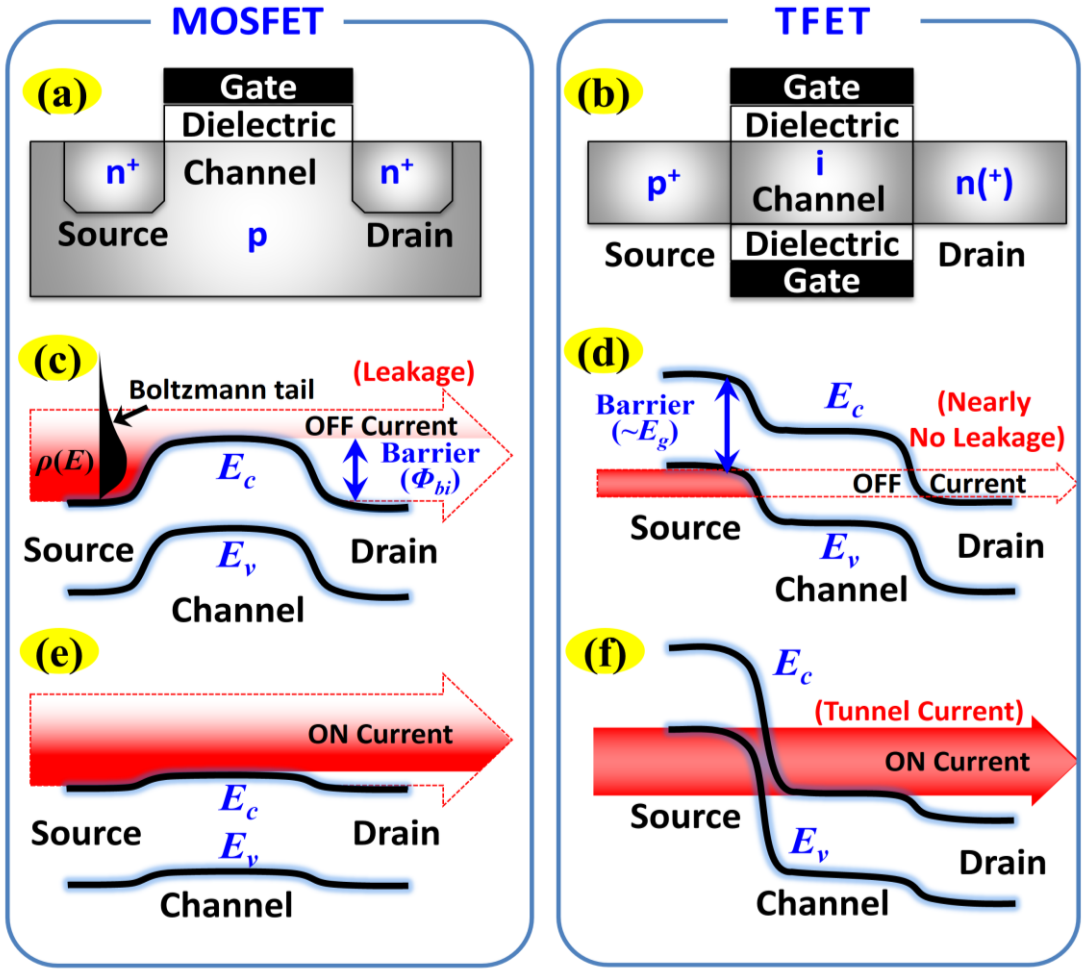


Figure 3: TFET vs. MOSFET.

Schematic of (a) a typical MOSFET and (b) a typical double-gated TFET; Band diagram and current of (c) MOSFET and (d) TFET in OFF state; Band diagram and current of (e) MOSFET and (f) TFET in ON state. The red arrows indicate direction of electron movement.

As conventional FETs (**Figure 3a**) approach their limits in controllability of power consumption (mainly due to the "Boltzmann tail" that causes OFF-current, as shown in

Figure 3c, Tunnel-FETs (TFETs) (**Figure 3b**) are considered as promising candidates for a range of electronic applications including ultra-low-power computing, as well as ultra-sensitive bio sensors or gas sensors **[45]**. TFETs employ the tunneling of electrons/holes through the semiconductor band gap (E_g) **[46]** (**Figure 3d,f**) and can switch ON/OFF with subthreshold swing (*SS*) smaller than 60 mV/dec.

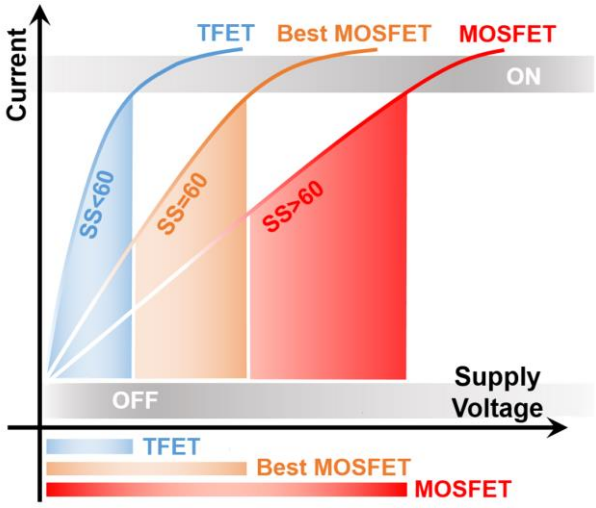


Figure 4: Illustration showing steep turn-on of TFET at low supply voltage

Nano-scale TFETs based on conventional 3D materials have a severe scaling issue that the E_g's vary uncontrollably with the bulk thickness (in nm scale) and thereby cause variations in tunneling currents. However, 2D materials have intrinsic thickness of a few Å/layer (as discussed in **Section C**), and controllable precise band gaps as a function of # of layers, which enable the scaling of TFETs without inducing performance variations. TFETs based on graphene may also utilize the band gap tunability by width variation of graphene to achieve high ON-OFF ratio (I_{ON}/I_{OFF}). Moreover, 2D materials have further advantages in terms of device topology, which benefits from excellent electrostatics and thus high ON-current (I_{ON}, tunneling current in ON state). In addition, the pristine interfaces of 2D

materials without dangling bonds can prevent TFETs from being influenced by the interface states (as discussed in **Section C**). Besides, while the 3D density of states (DOS) varies as square root of energy and limits the most optimal design of TFETs, 2D DOS is constant or linear (in case of graphene) with energy, which allows more abrupt turn-on in TFETs. Hence, 2D materials, exhibit high potential for building TFETs **[47]**.

One of my contribution works have shown that heterostructures of 2D materials can provide better performance and energy efficiency w.r.t 3D materials based TFETs **[48]**. Moreover, I have contributed to the demonstration of the first 2D-Channel TFET based on 2D-3D vertical heterostructure, which is the only TFET to achieve *subthermionic SS* over four decades of drain current, at V_{DD} of 0.1 V **[9]**. Such novel tunnel devices uniquely enabled by 2D materials can open up unprecedented opportunities for next generation ultra energy-efficient electronics.

3. Technology Scaling – Interconnect and Passives

Copper (Cu) interconnects suffer from significant size-effect at aggressively scaled technology nodes, leading to a rapid increase of resistivity and more severe self-heating that degrades interconnect electromigration (EM) reliability and thereby limits its current carrying capacity **[15], [49], [50]**. Use of other metals, including W **[51]**, Ru **[52]**, Mn **[53]**, Co **[54]**, etc., alleviates the EM reliability issue, but reduces interconnect electrical conductivity and, eventually, suffers from the same current carrying capacity limitation.

Therefore, a new material is desired to overcome this issue. Graphene ribbon/nanoribbon (GR/GNR) is known for its extremely high current carrying capacity (> 100 MA/cm^2) **[55], [56]**, and its strong sp^2 covalence bonding promises excellent EM resistance, compared with metals (e.g. Cu). Additionally, the superior in-plane thermal conductivity of ML-graphene w.r.t. conventional interconnect materials can be exploited to alleviate on-chip hot spots, and

further improve reliability. According to theoretical studies, the electrical conductivity of multilayer (ML-)GNR can be enhanced by intercalation doping **[57]**. Recently, our $FeCl_3$ intercalation doped ML-GNR interconnect (of width down to 20 nm) was reported to beat Cu in performance and energy efficiency **[15]**. The intercalation doped ML-GNR also shows excellent reliability performance in terms of current carrying capacity, w.r.t. Cu, and is a promising candidate for the next generation interconnect material **[16]**.

Resistors, capacitors, and inductors are the three most basic elements used in electronic circuits, each of which plays an important role in how an electronic circuit behaves. Inductor provides the "inductance" characteristic in analog and radio-frequency electronics. On-chip inductors represent a broad technology relevant to many important applications, such as wireless communications, sensing, and energy storage and transfer. Integration of the inductors into semiconductor chips can greatly benefit the cost, power, design flexibility, size, reliability, and tolerance of electronic hardware, which is a significant portion of the *Internet of Things and Industry 4.0*.

Unlike the continuous scaling of transistors and interconnects in the IC technology achieved with increase in performance, progress toward miniaturization of passive devices especially on-chip inductors has remained elusive mainly due to the fact that large inductor areas, dictated by fundamental electromagnetics, are required in order to deliver the desirable inductance values and performance targets.

Theories have identified that carbon nanomaterials including carbon nanotubes and multilayer graphene (MLG) can be a very attractive material-based approach for on-chip inductors **[58], [59]**, because the large momentum relaxation time (τ) of low-dimensional carbon allotropes could lead to large *kinetic inductance*, thus contributing to high area-efficiency and performance, as well as immunity to skin effect **[60], [61]**.

4. Transparent Electrode for Optoelectronic Devices

Single layer graphene is a highly transparent material with a typical optical transparency of ~97.5% **[62]** and absorbs less than 0.1% of the incident light in the visible region of the spectrum. In few layer graphene, each layer of graphene can be considered as a 2D electron gas. With some approximation **[62], [63]**, the transparency of graphene becomes T=100%-2.3%×N, where N is the number of layers. The absorption spectrum shows a peak around wavelength of 270 nm in the ultra-violet region, and remains relatively flat in visible range (400 – 700 nm) extending to 2500 nm wavelength.

As the cost of the commonly used transparent electrode material Indium Tin Oxide (ITO) increases, high transmittance, high conductivity, high mechanical flexibility as well as impermeability to moisture (leading to improved reliability) make graphene a promising electrode material for a variety of photovoltaic applications **[10]**, such as touch panels, displays, light emitting devices, light sensors and solar cells. In fact, graphene electrode has already been widely integrated in photovoltaic cells with organic semiconductors **[64]–[66]**, n-silicon **[67]**, CdS nanowire **[68]**, CdTe **[69]** and ZnO **[70]** to replace ITO.

5. Electrocatalytic Devices for Renewable Energy

Hydrogen has been widely considered as a promising alternative and renewable energy to replace fossil fuels **[71]–[73]**. Toward this end, the direct and efficient approach for massive hydrogen production is to split water using electrocatalytic hydrogen evolution reaction (HER) **[74], [75]**. The most active electrocatalysts for HER is Platinum (Pt), which can drive HER with a near zero overpotential **[76], [77]**. However, the scarcity and high costs of Pt significantly restrict its applications in large scale. It remains challenging to develop highly active HER catalysts based on the materials with more abundance and lower cost compared with Pt **[78]–[80]**. Recently, MoS_2, one of the transition metal

dichalcogenides (TMDs), has drawn considerable attention in HER due to the excellent stability and earth abundance **[81]–[85]**. Pt nanoparticles decorated MoS_2 synthesized on Mo foil (i.e. Pt/MoS_2/Mo) hybrid catalyst demonstrates high HER electrocatalytic activity with low overpotential and small Tafel slope, which is much beyond previous reported works using MoS_2 and is close to the upper-limit values of HER achieved on Pt electrode **[14]**.

C. Integration Challenges

The increasing need of electronic devices discussed above, provide opportunities for many 2D materials. While use of 2D materials can provide not only improved dimensional scalability, but also unique electronic applications, however, building of 2D material based device itself faces several problems.

Challenges in applications of 2D materials in electronic devices and circuits include material preparation (synthesis, transfer, and patterning) contact, interface and doping. Especially, the parasitic contact resistance between metal electrodes and 2D materials is another key factor in device/circuit applications that demands careful attention. Moreover, achievement of integration all the process is a daunting challenge.

1. Metal Contacts

The functioning of all semiconducting electronic devices is based on the fine control over the flow of charge carriers injected into the semiconducting material through electrical contacts. The quality of electrical contacts, quantified through contact resistance, is as important to the proper functioning of the entire device as the semiconductor itself. Since the early 90s, researchers have explored a wide variety of electronic devices based on nanostructures with different dimensionality, ranging from 1D carbon nanotubes **[86]**, semiconductor nanowires **[87]** or 2D materials starting with graphene **[88]**.

One of the most common electronic devices, both in the research and industrial environment is the field-effect transistor (FET). Low contact resistance in these devices based on 2D semiconductors is critical to achieving high ON currents, high photoresponse **[89]** or high-frequency operation **[90]**. However, the major issue for 2D semiconductor-based transistors is the existence of a large contact resistance, which drastically restrains the drain current **[91]–[93]**. Contacting 2D semiconductors presents a certain number of experimental and conceptual challenges. The theoretical concepts underlying our understanding of contacts break down in the limit where the semiconductor thickness is smaller than the depletion and transfer lengths. In the 2D limit, the properties of the interface, that is the chemical interaction between the metal and the semiconductor governs everything. The pristine surfaces of 2D materials (without dangling bonds) make it difficult to form strong interface bonds with a metal, and thereby increase contact resistance.

2. Other Interfaces

The carrier mobilities extracted from 2D materials in electronic devices are always much lower than their theoretical values, including the on impurity **[94]** and phonon limited mobilities **[95]**. Such low mobility greatly limits the drive current as well as the switching speed of MoS_2 devices, induce more variations and remains an essential issue.

This phenomenon is caused by several interface issues which are almost inevitable, such as the interaction between the 2D material and its surrounding materials (substrates and dielectrics), as well as grain boundaries in 2D material itself that act as imperfection sites inducing extra scattering and varations. In 3D materials, these issues cause less problem than in 2D, since in 2D there is only one or few single atomic layers and every interface becomes essential.

3. Doping

For various applications including FETs and photovoltaics, it is necessary to tune the electronic properties of TMDs through modulation of the mobile charge concentrations, or, in other words, doping.

Ion implantation, a common strategy adopted to decrease the contact resistance in bulk semiconductors is not applicable for 2D materials, because their ultra thin body cannot sustain the damage from ions. Hence, exploration of efficient doping methodologies are required, which would be stable, easy to implement and would not lead to significant defects in the 2D materials.

D. Synopsis of the Dissertation

In the following chapters, I will carry out detailed analysis of these issues and I will propose and demonstrate solutions to address them. It is also illustrated in this dissertation, that the novel approaches proposed here, can be leveraged to demonstrate completely different device technologies.

In **Chapter II**, as the background of this dissertation, 2D materials are systematically explained, including their fundamental physics, their unique properties and their synthesis methods.

Chapter III explores the metal contacts to 2D materials. The chapter provides in-depth physical understanding of the fundamentally different charge injection mechanisms which lead to the contact resistance issue. The first detailed methodology for the accurate evaluation of metal contacts to 2D layered materials is presented. Approaches are demonstrated for reducing such contact resistance and improving the performance of the transistors based on 2D semiconductors.

Chapter IV explores more interface issues with 2D materials, such as 2D materials'

interfaces with dielectrics, substrate and other bulk semiconductors, as well as grain boundaries inside 2D itself. In the last of the chapter, interface engineering is explored for steep transistors which are relatively less disruptive compared to present CMOS technology.

In **Chapter V**, in order to realize many electronic devices based on 2D materials, an important process – doping is investigated and critical strategies are demonstrated for fabrication of various devices, such as transistors interconnects, inductors and electrocatalyst devices.

Based on the intercalation doping method studied in **Chapter V**, **Chapter VI** presents the first exploitation of the unique properties of intercalated-graphene in RF electronics – specifically the first demonstration of on-chip inductors based on intercalated-graphene, with extraordinary benefits compared to conventional counterparts.

In **Chapter VII**, Gate-induced drain leakage (GIDL) in 2D FETs is evaluated for the first time, using a novel quantum transport methodology. It is shown that certain 2D semiconductors can greatly reduce GIDL. Material properties and device geometry are also discussed, which provide guidelines for study of low-leakage 2D FETs.

Chapter VIII provides the conclusions and directions for future work.

II. Fundamentals of 2D Materials

A. Graphene Physics

1. The Rise of Graphene

Carbon is the fourth most abundant element in the universe by mass (after hydrogen, helium and oxygen). In human body, carbon takes up about 18.5% of the weight, ranking second after oxygen **[96]**. This abundance, together with the unique diversity of organic compounds and their extraordinary ability to form polymers at common temperatures on Earth, make this element the chemical basis of all known life forms.

In a carbon atom, the 4 valence electrons can combine with that of other carbon atoms in a variety of ways (termed as sp^2, sp^3, etc). Hence, by distinct types of valence bonds, carbon atoms can form various allotropes**,** varying among three-dimensional (3D), two-dimensional (2D), one-dimensional (1D) and zero-dimensional (0D) materials, as shown in **Figure 5**.

3D Diamond, which had been discovered in India since 3000-6000 years ago, is a metastable allotrope of carbon with carbon atoms arranged in face-centered cubic lattices. It is an insulator. In 1772, Antoine Lavoisier showed that the only product of diamond burnt under concentrated rays of sun was carbon dioxide, proving that diamond is composed of carbon **[97]**.

As with diamond, graphite is also a historical 3D solid allotrope of carbon, but a conductor. Graphite has been used by people since the Neolithic Age (about 400 B.C.) in southeastern Europe **[98]**, but it was not until 1789 that it was named as “graphite” (meaning “writing stone”) by Abraham Gottlob Werner. It is the most stable form of carbon and is a semimetal native element mineral. Graphite has a layered, planar structure as shown in **Figure 5**. In each layer, the carbon atoms are covalently bonded and arranged in a

honeycomb lattice while adjacent layers are held together by relatively weak van der Waals (vdW) bonds.

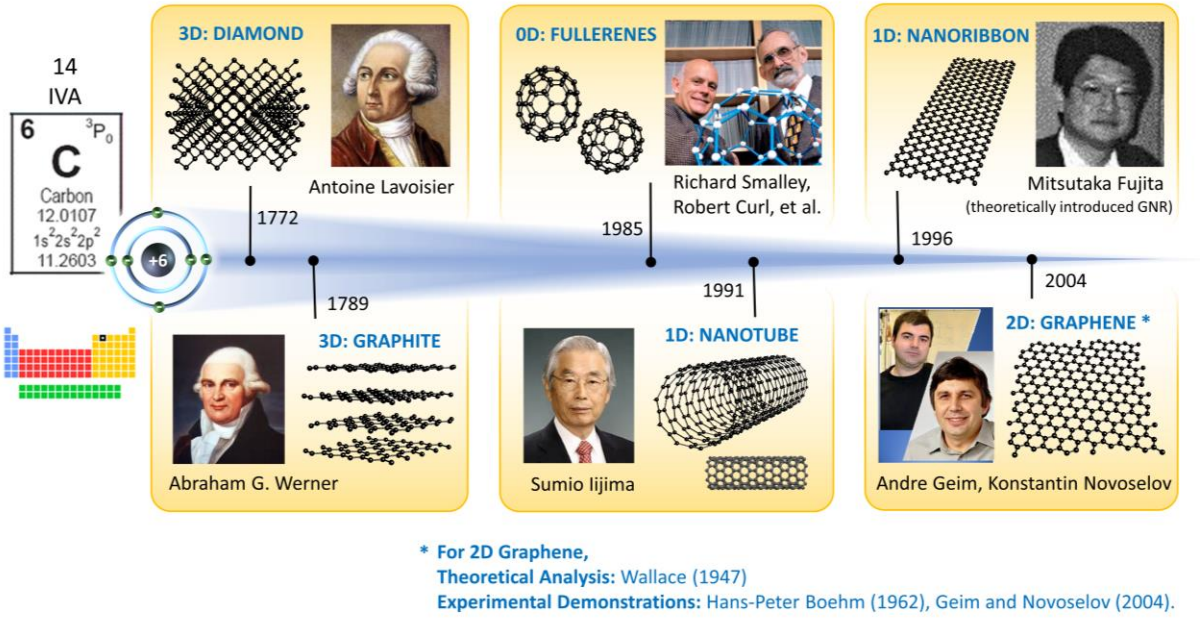


Figure 5: History of Carbon allotropes.

Left: fundamental information (group: 14/IVA; atomic number: 6; ground-state level: $^3P_0$; atomic weight: 12.0107; ground-state configuration: $1s^2 2s^2 2p^2$; Ionization energy: 11.2603 eV) of carbon element in the periodic table; Right: different allotropes of carbon (diamond/ graphite/ fullerenes/ nanotube/ nanoribbon/ graphene) with their brief history.

Other than amorphous carbon allotropes such as soot and charcoal, other molecule and crystal allotropes can be found as well. In the past 30 years, low-dimensional (2D, 1D and 0D) carbon allotropes have been discovered in successions, although in an order (from 0D to 2D) that is exactly reverse of low-D structures artificially-fabricated with conventional semiconductors (from 2D quantum wells, 1D quantum wires and 0D quantum dots). 0D

Fullerenes (such as buckminsterfullerene, C_{60}) (**Figure 5**), which are molecules composed entirely of carbon in the form of hollow spheres, ellipsoids or cylinders, were first experimentally prepared in 1985 by Richard Smalley, Robert Curl, et al., at Rice University, though Fullerenes have also been found in nature in 1980s-1990s **[99], [100]**.

Carbon allotropes with one-dimensional (1D) tubular nanostructures – carbon nanotubes (CNTs) (**Figure 5**) were then discovered by Sumio Iijima of NEC in 1991. Rigorously speaking, CNTs are categorized as a member in the Fullerenes family, which are considered as cylindrical Fullerenes with high length-to-diameter ratio of up to 132,000,000:1 **[101]**. CNTs are the strongest materials discovered till date in terms of tensile strength and elastic modulus. CNTs can be either semiconducting or metallic depending on their structures, a property known as chirality **[61]**.

The experimental demonstration of 2D graphene, a carbon allotrope composed of a truly one-atom thick layer of carbon atoms (**Figure 5**), by Novoselov et al. **[88]** in 2004, has opened up a new era. The term graphene was coined as a combination of graphite and the suffix *-ene* by Hanns–Peter Boehm **[102]**, who had also described single-layer carbon foils in 1962 **[103]**. This atomically-thin crystal can be easily prepared by the micromechanical exfoliation of the layered 3D graphite. In the nanoelectronics community, graphene, as well as nanostructures derived from graphene (such as graphene nanoribbon (**Figure 5**)), have drawn the most attention so far and have triggered the highest number of research efforts among all low-dimensional nanomaterials, because of its fascinating properties that are promising for electronic and optoelectronic devices.

In this section, an overview of the essential physics from atomic point of view and the key/unique electronic applications of graphene are provided to highlight its role in emerging nanoelectronics, optoelectronics, flexible electronics and other technology sectors such as

energy and sensing. Challenges of graphene applications are reviewed as well.

2. Crystal and Electronic Structures

Carbon is the sixth element in the periodic table, which means that there are six electrons surrounding the atomic core, arranged in $1s^2 2s^2 2p^2$ configuration (**Figure 5**). Since the two $1s^2$ electrons remain very close to the core, the carbon allotropes are all bonded by various combinations of the four $2s^2 2p^2$ orbital valence electrons of each carbon atom.

In 3D diamond, each of the four valence electrons in one carbon atom is shared with one of the four neighboring carbon atoms, same as that in silicon. However, in 2D graphene, a carbon atom shares electrons with three nearest neighbors (**Figure 6a,b**), in the form of three sp^2 bonds, forming a honeycomb-like hexagonal lattice. The sp^2 bonding (with 120 degree angle) is responsible for the planar and hexagonal structure of graphene. It is worth noting that such honeycomb structure is the basic structural element of other allotropes as well, including graphite, carbon nanotubes and fullerenes.

The three electrons forming the strong sp^2 bonds are responsible for the outstanding mechanical and thermal properties of graphene. However, other than the sp^2 bonds, there are also out-of-plane p_z orbitals with one electron per atom, as shown in **Figure 6b**, which are responsible for the electrical conduction of graphene.

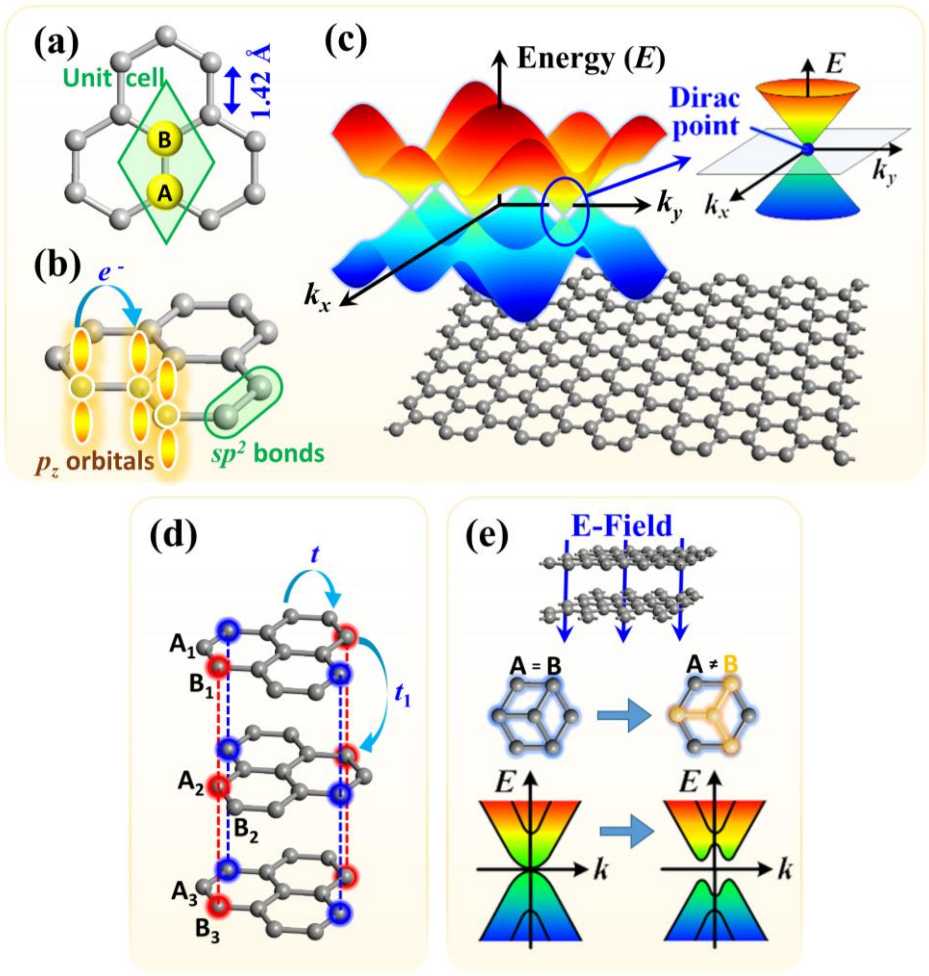


Figure 6: Physics of graphene.

(a) Lattice structure of graphene (A and B are the two 'basis' of graphene's crystal structure); (b) bonds and orbitals of graphene; (c) *E-k* dispersion of graphene; (d) lattice structure of ABA stacking few layer graphene; (e) schematic views and *E-k* dispersion of AB stacking bilayer graphene without (left) and with (right) vertical electric field.

The electrons in the p_z orbitals of graphene can easily hop between the neighboring atoms. The hopping energy (energy characterizing the hopping) is ~3.0 eV, which indicates a large overlap of the Hamiltonians of the neighboring atoms and thus delocalized electron

wavefunctions. These electrons contribute to the outstanding electrical properties, and form the π bands in the conduction bands (E_c) and π* bands in the valence bands (E_v) of graphene. Based on tight-binding method, the electronic structure $E(\boldsymbol{k})$ (the dispersion relation that expresses E of the carriers as function of wave vector, $\boldsymbol{k}$) is given by the equation:

$$\hbar v_F \left(\boldsymbol{\sigma} \bullet \boldsymbol{k}\right)\left|\psi\right\rangle = E\left(\boldsymbol{k}\right)\left|\psi\right\rangle \tag{2}$$

where v_F is a constant group velocity $v_F = 3ta/2 = 10^6$ m/s; $\boldsymbol{k} = (k_x, k_y)$ is the wave vector; $\boldsymbol{\sigma} = \boldsymbol{x}\,\sigma_x + \boldsymbol{y}\,\sigma_y + \boldsymbol{z}\,\sigma_z$ is composed by Pauli matrices. $E(\boldsymbol{k})$ is then obtained as **[104], [105]**:

$$E\left(\boldsymbol{k}\right) = E_F \pm t\left[3 + 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right)\right]^{1/2} \tag{3}$$

where ± represents π and π* bands, respectively. t (~ 3 eV) is the nearest-neighbor hopping energy; a (~1.42 Å) is the C-C bond length; E_F is the Fermi level of graphene. For intrinsic graphene, E_F ~ 4.5 eV.

As shown in **Figure 6c**, at the six corners of the first Brillouin zone, where $k = (0, \pm 4\pi/3a)$, $k = (\pm 2\pi/3a, \pm 4\pi/\sqrt{3}a)$, or $k = (\pm 2\pi/3a, \mp 4\pi/\sqrt{3}a)$, $E(k) = E_F \pm 0$ can be found, meaning that E_c (π bands) and E_v (π* bands) meet at the six points resulting in a zero band gap. Since the Hamiltonian in (2) is more similar to the Dirac equation than the Schrodinger equation, these six corner points are named as Dirac points. Moreover, near the Dirac points, by approximately expanding $E(\boldsymbol{k})$, linear E-k dispersions are found as:

$$E\left(k\right) = \pm \hbar v_F k \tag{4}$$

Hence, to calculate the effective mass, the traditional definition of the carrier effective mass $m^* = [(1/\hbar^2)(d^2E/dk^2)]^{-1}$) for parabolic dispersion should not be applied. Instead, the effective mass can be calculated using the momentum p:

$$m^* = \frac{p}{\partial E / \partial p} = \hbar^2 k\left(\frac{\partial E}{\partial k}\right)^{-1} \tag{5}$$

By applying (5) to $E(k) = \hbar v_F k$, the effective mass of carriers in graphene can be calculated as $m^* = \hbar k / v_F$, for both electrons and holes. Hence, the effective mass near the Dirac points (k~0) is nearly zero.

In summary, graphene behaves like a semi-metal **[88]** with ultra-low and equal electron/hole effective masses, and ultra-high electron/hole mobility (See **Table 1**).

Table 1: Properties of carbon nanomaterials.

Single-walled CNT (SWCNT), multi-walled CNT (MWCNT), and graphene are included in comparison to those of some semiconductors (Si, GaAs, and GaN) and metal (Cu) used for various electronics applications.

Properties	Si	GaAs	GaN	Cu	SWCNT	MWCNT	Graphene
Max current density (A/cm^2)	-			10^7	$>1x10^9$ **[106]**	$>1x10^9$ **[107]**	$>1x10^8$ **[88]**
Melting point (K)	1687	1513	2773	1356			3800
Tensile strength (GPa)	7	75	204	0.22	22.2±2.2	11-63	
Mobility (cm^2/V-s)	1400	8500-9500	1100		>10000		>10000
Thermal conductivity ($\times 10^3$ W/m-K)	0.15	0.055	0.13	0.385	1.75-5.8 **[108]**	3.0 **[109]**	3.0-5.0 **[110]**
Temperature coefficient of resistance (10^{-3} /K)	-			4	<1.1 **[111]**	-1.37 **[112]**	-1.47 **[113]**
Mean free path (nm) (room temperature)	30	~ 300	~ 20-30	40	>1,000 **[114]**	25,000 **[115]**	~1,000 **[116]**

3. Carriers in Graphene

Based on the E-k dispersion, the density of states (DOS) of graphene is given by $g(E) = 2|E|/\pi(\hbar v_F)^2$, which is linear in energy. The charge carrier densities in graphite are almost equal for electrons and holes (7×10^{18} cm^{-3}). The Hamiltonian for carriers with energy near

the Dirac point can be written as,

$$\hat{H} = \pm\hbar v_F \sigma \cdot k = \pm\hbar v_F \begin{bmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{bmatrix} \quad (6)$$

where σ is the 2D Pauli matrix, referring to pseudospin, which is used to indicate the respective contribution of *A* and *B* atoms (shown in **Figure 6a**) in graphene to the electronic states near the Dirac point, rather than the real spin of carriers. States in the conduction and valence bands of graphene are described by the same spinor wave function, leading to the symmetry between electrons and holes.

The symmetry between electrons and holes can also be found in the chirality **[117]** in quantum electrodynamics (QED). The chiral symmetry leads to many QED-like phenomena, such as anomalous quantum Hall effect **[118], [119]**, Hofstadter's butterfly **[120], [121]**, Klein paradox **[122]–[124]**, absence of localization and thus metal-insulator transition **[125], [126]**, and finite minimum conductivity **[118], [127]**.

It is worth mentioning that the observed fractional quantum Hall effect in graphene greatly enriched the physics of Hall effect which has already rendered several Nobel prizes in history. Due to the linear E-k relation of the Dirac cones, the Landau energy levels (the orbits with discrete energy values that can be occupied by charged particles in magnetic fields) in graphene is found to be **[128]**,

$$E_n = \frac{n}{|n|}\sqrt{2e\hbar v_F^2 |n| B} \quad (7)$$

where *n* is an integer index (positive for electrons, negative for holes), *e* is the charge of an electron, and *B* is the magnetic field that should be applied normal to the graphene plane during the Hall conductance measurement. Compared to the conventional semiconductor quantum well, graphene displays a symmetric Landau level distribution for electrons and holes, non-uniform Landau level separation, and non-zero states at zero-energy level ($n = 0$),

which may lead to new applications in carbon based electronic and magneto-electronic devices.

Hofstadter's butterfly – a stunning fractal pattern that describes the behavior of electrons in a magnetic field – has been recently measured experimentally for the first time in graphene **[120], [121]**. By placing graphene on the surface of hexagonal boron-nitride (h-BN), "Moiré patterns" can be observed, which are regular patterns created whenever two similar 2D lattices are overlaid. Then the energy spectrum of the superlattice can be determined by measuring its electrical conductivity in strong magnetic fields. The Hofstadter butterfly first predicted in 1976 **[129]** were seen in the plotted electron density versus magnetic field strength **[120], [121]**.

4. Optical Properties

Graphene also has interesting optical properties. The application of ultra-fast optical pulses to graphene leads to inter-band excitations and produces a non-equilibrium carrier population in the valence and conduction bands. Two relaxation time scales of ~ 100 fs (due to carrier-carrier intra-band collision and phonon emission) and ~ 1 ps (due to electron inter-band relaxation and cooling of hot phonons) are observed **[130]–[132]**.

Single layer graphene is a highly transparent material with a typical optical transparency of ~97.5% **[62]** and absorbs less than 0.1% of the incident light in the visible region of the spectrum. In few layer graphene, each layer of graphene can be considered as a 2D electron gas. With some approximation **[62], [63]**, the transparency of graphene becomes T=100%-2.3%×N, where N is the number of layers. The absorption spectrum shows a peak around wavelength of 270 nm in the ultra-violet region, and remains relatively flat in visible range (400 – 700 nm) extending to 2500 nm wavelength.

5. Bilayer and Few Layer Graphene

Bilayer graphene and few layer graphene are stacks of two and several graphene layers, respectively. The band structure of bilayer or few layer graphene is described by a Hamiltonian similar to that of graphite. The tight-binding description takes into account the in-plane hopping energy between carbon atoms (t ~ 3 eV **[133]–[135]**, the nearest-neighbor hopping energy between *A* and *B* atoms in one plane, as shown in **Figure 6d**) as well as the inter-layer hopping energies (t_1 ~ 0.39 eV **[133]–[135]**, represents the interaction of atoms *A* and *B* in adjacent layers). Bilayer and few layer graphene are shown to have a zero band gap as that of monolayer graphene, but with a near-parabolic dispersion near the Dirac point (**Figure 6e**).

Different stacking of graphene layers leads to a variety of different electrical properties **[134], [135]**. The stacking of interest is the Bernal stacking (AB or ABA) due to its dominant distribution in natural graphite and highly oriented pyrolithic graphite (HOPG). The graphene band structure is sensitive to the lattice symmetry (the symmetry between A and B, as shown in **Figure 6e**). A band gap can be opened in AB stacking bilayer graphene by applying an electric field perpendicular to the layers **[136]** (**Figure 6e**). In such case, the potential difference between the layers leads to an intralayer potential difference between the basis A and B in the hexagonal structure, resulting in the formation of a gap between π and π* states **[137]** (**Figure 6e**). Similarly, the electric field can also open up a small band gap in ABC stacked tri-layer graphene **[138]**. Markedly differently, ABA stacked tri-layer graphene is a semimetal with a resistivity that decreases with increasing electric field **[138], [139]**.

6. Graphene Nanoribbons

Graphene nanoribbons (GNRs) were originally introduced as a theoretical model by

Mitsutaka Fujita, et al. in 1996 to examine the edge and nanoscale size effect in graphene (**Figure 5**). GNRs generally refer to graphene patterned into narrow strips (width w < tens of nm) (**Figure 7a**,**b**), which has a spatial confinement along the width, and thereby has a band gap, as shown in **Figure 7c**.

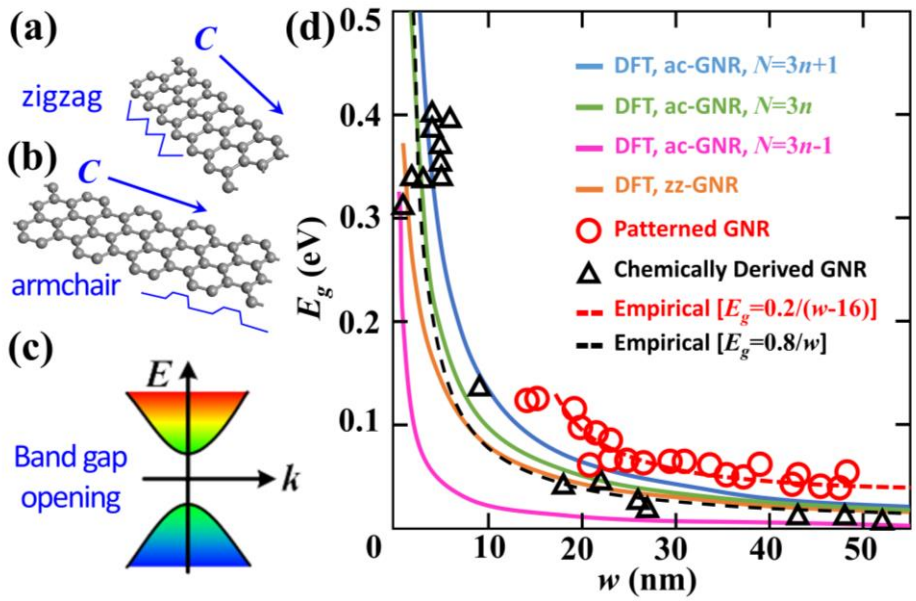


Figure 7: Physics of GNR.

(a, b) Chiralities of GNR; (c) typical band structure of GNR; (d) Band gap (E_g) vs. width (w) for GNRs, including density functional theory (DFT) calculated results [140] and measured results of chemically derived GNRs [141] and lithographically patterned GNRs [142]. N is the number of carbon atoms along the width direction.

The arrows in **Figure 7a,b** show the vector along the length direction, which is also the typical direction of transport in a GNR. The vector is defined as $C = n\,a_1 + m\,a_2$, where a_1 and a_2 are the lattice vectors of graphene, and n and m are the chiral indexes. As such, the chiral indexes (n,m) uniquely define the "chirality," or the direction of the transport. For the

GNR in **Figure 7a**, $C = n\ a_1 + 0\ a_2$, and hence, the chirality is identified as (n, 0). In this case, because the edge of GNR has a zigzag shape (shown in blue), it is also called a zigzag GNR (zz-GNR). Similarly, for the case shown in **Figure 7b**, the GNR is identified with the chiral indexes (n, n), and because the edge has armchair shape, it is called an armchair GNR (ac-GNR).

Opening up a band gap in graphene is a key topic of interest aiming at digital applications. The wave function along the GNR width vanishes at the two edges. Thus, the wave vector quantization in GNR is $w\ k = \pi i$, where w is the width of GNR, and i is an integer. Armchair GNRs (ac-GNRs) are semiconducting, due to both the quantum confinement and the crucial effect of the edges **[140]**. zz-GNRs also have band gaps because of the staggered sublattice potential from magnetic ordering once electron spin is considered **[140], [141]**. The calculated band gap of GNRs increases with decreasing ribbon width, however, in four curves corresponding to different chiralities (ac-chirality with N=3n-1, ac-chirality with N=3n, ac-chirality with N=3n+1 ac, and zz-chirality, where N is the number of carbon atoms along the width direction, and n is a positive integer) **[140]**, as shown in **Figure 7d**. Due to the edge roughness, experimental GNRs always have an increased band gap with decreasing width regardless of chirality, described by an empirical expression of $E_g \sim \alpha / w$ eV **[141]** or $E_g \sim \alpha / (w\text{-}w_0)$ eV **[142]**, where a is a constant to be fitted (**Figure 7d**).

However, the current bottom-up and top-down synthesis technologies of GNRs are still under improvement. Especially, top-down GNRs usually suffer from edge roughness, while bottom-up GNRs are lack of the controllability in terms of dimensions and positions. Some nanostructures derived from graphene other than GNR can also own a band gap, such as graphene nanomesh **[143], [144]** and graphane **[145], [146]**.

However, the demonstrations of other novel 2D semiconductors, including transition-

metal dichalcogenides (TMDs) (such as MoS_2 **[23], [147]**), black phosphors **[29]**, etc., open up a new "beyond-graphene" era. These materials have intrinsic band gaps and are considered as promising candidates for digital electronics in the next generation.

B. 2D Materials Beyond Graphene

The demonstration of graphene has truly built up a new stage for a wide range of 2D materials and their electronic applications. For example, hexagonal boron nitride (h-BN) has similar lattice structure as graphene, but has a large band gap (E_g >5 eV) and can be used as an ultra-thin dielectric. Similarly, layered TMDs such as MoS_2 **[23]**, WSe_2 **[25]**, WS_2 etc have attracted tremendous attention due to their semiconducting attributes with band gaps in the range of 1–2 eV. Availability of these 2D materials with such wide range of band gaps can not only open up new vistas for electronic and photonic device applications but also facilitate exploration of novel heterostructure devices formed by combining (both laterally and vertically) such 2D atomic crystals **[148]**.

In this section, a new and systematic taxonomy is proposed for 2D materials. Then the most important group in this dissertation – the TMD group will be introduced in more details.

1. 2D Material Groups

The first method to category 2D materials is by their crystal structures. As shown in **Figure 8**, one can classify 2D materials into five main groups:

i. Group IV (also includes Group III-V). Members other than graphene in Group IV typically have very similar properties to graphene – zero band gap, linear *E-k* disperstion and high mobility. While Group III-V are typically insulators, such as hexagonal BN (hBN).

ii. Group IV Derivatives: This group is derived from Group IV, by chemical decoration

of hydrogen or halogen atoms or some atomic groups. They are typically low band gap semiconductors with high mobilities.

Table 2: Examples of 2D materials classified by conductivity.

	Metals	Semiconductors	Insulators
Group IV (III-V)	C, Si, Ge, Sn, Pb	SiC	BN
Group IV derivatives		CH, SiH, GeH, $GeCH_3$, SnH	CF
TMD	NbS_2, $NbSe_2$, TaS_2, VO_2	MoS_2, WSe_2, $SnSe_2$	
Group III-VI		GaS, GaSe, InS, InSe	
Group V (IV-VI)		P, Ar, SnS, SnSe, GeS, SiS	
Others	Mo_2C, WC, Ti_2CX_2,ZrNCl	Bi_2Se_3, cobaltites	MoO_3, $Ni(OH)_2$,

iii. Transition Metal Dichalcogenide (TMD) Group have three atomic planes in each layer. They are typically semiconductors or metals. This class of materials has a common chemical formula MX_2 where M stands for a transition metal (most commonly Mo, W, Nb, Ta, Ti) and X a chalcogen atom (S, Se, Te). Compounds based on Mo and W are the best known examples of semiconducting TMDs. Semiconducting TMDs usually have large band gaps, intermediate effective masses and intermediate mobilities.

iv. Group III-VI is a group very similar to TMD Group, but with four atomic planes in each layer. They typically have similar properties to TMD Groups as well.

v. Group V (and Group IV-VI) are typically semiconductors with high mobility. However, all of this group are anisotropic materials, i.e. the effective masses and mobilities

are very different among different transport directions in the plane.

vi. Some other uncommon groups also exist, such as MXenes. They typically have more complex crystal structures than that of the five fundamental groups.

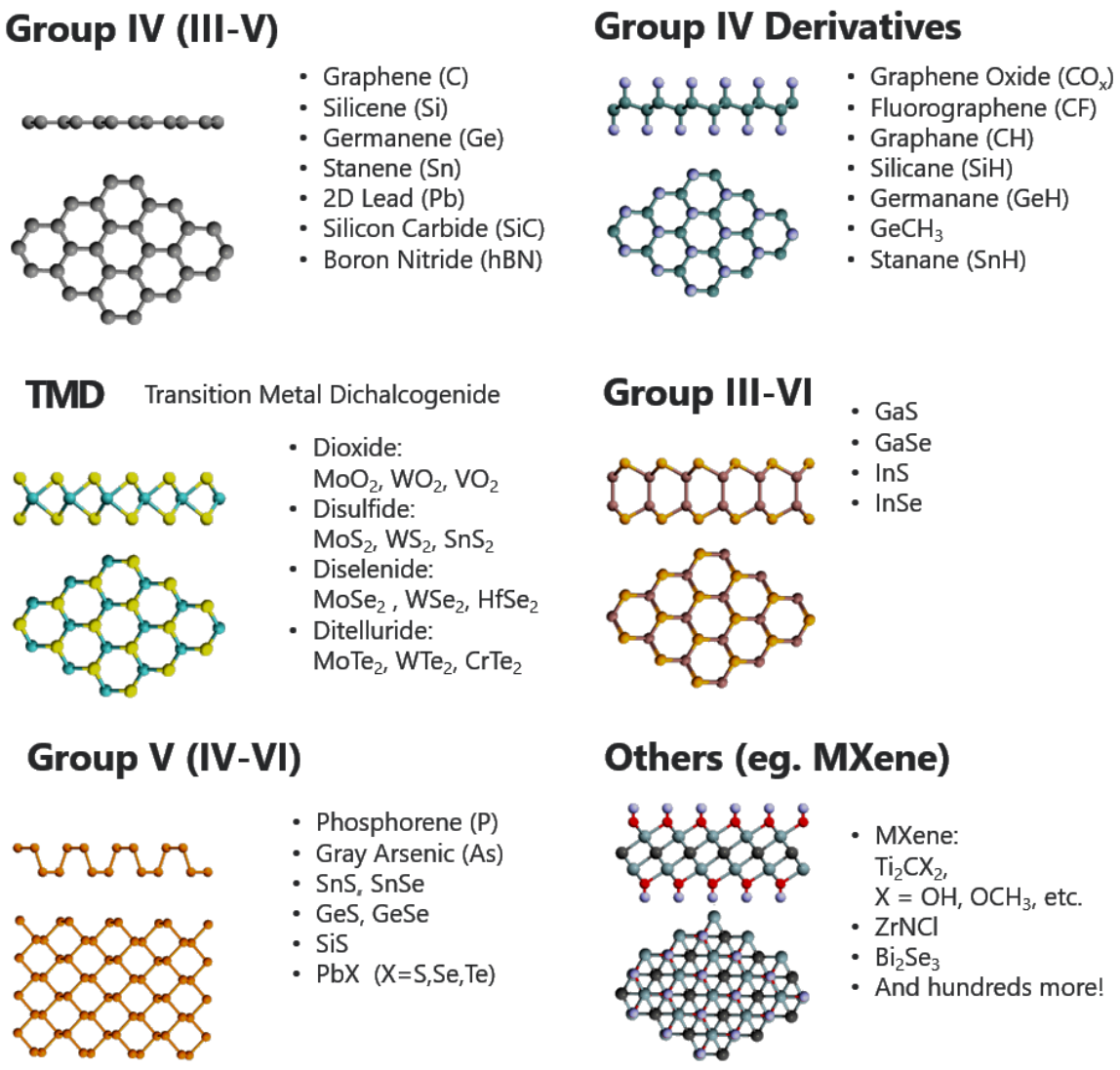


Figure 8: Classification of 2D materials by crystal structure.

One can also category 2D materials by their conductivity into three main groups: metals (including semi-metals and superconductors), semiconductors (including half metals) and

insulators, as shown by **Table 2**. Hence, 2D materials have very broad availabilities for electronic devices.

2. Transition-Metal Dichalcogenides (TMDs)

The in-plane lattice of TMD has two types of atoms, M and X, which are arranged in a 2D honeycomb array within the TMD plane, and in an X-M-X sandwich form normal to the TMD plane (**Figure 9**). M stands for *transition metal*, such as Mo, W, as well as Sc, Ti V, Cr, Mn, etc. X stands for *chalcogen*, including O, S, Se and Te. There are nearly 100 types of combinations. As in graphite, TMD layers are linked by weak Van der Waals bonds. The thickness of monolayer TMDs is typically ~0.7 nm, about two times that of graphene.

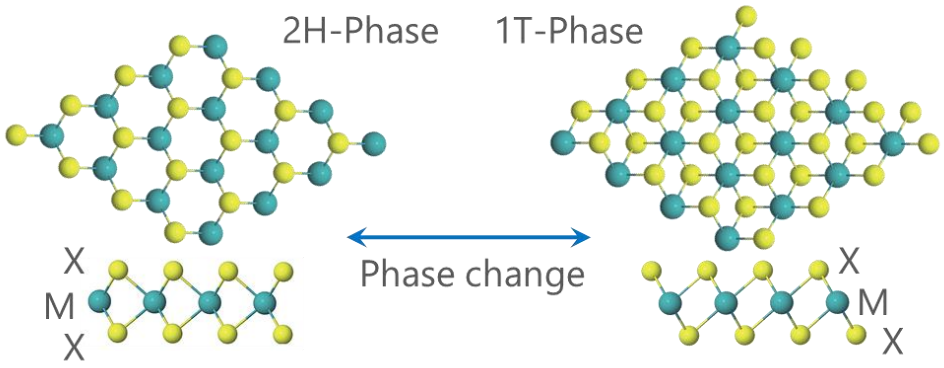


Figure 9: Two common crystal phases of TMDs (MX_2).

Figure 10 show the typical band structure of monolayer TMDs, in which the conduction band minimum and valence band maxima separate, and are both at the high-symmetry K point in the 1st Brillouin zone, as shown in **Figure 10**, i.e., monolayer TMDs have direct bandgaps, in contrast with bulk TMDs which have indirect bandgaps. The presence of finite band gaps in monolayer TMDs can be attributed to the lack of chiral symmetry. The

indirect-to-direct bandgap transition from bulk TMDs to monolayer TMDs is due to the spatial confinement along thickness direction **[27]**. The energy dispersions near the band edges are classic parabolic shape (**Figure 10**), indicating that carrier transport in monolayer TMDs can be described by the effective mass based Schrodinger equation.

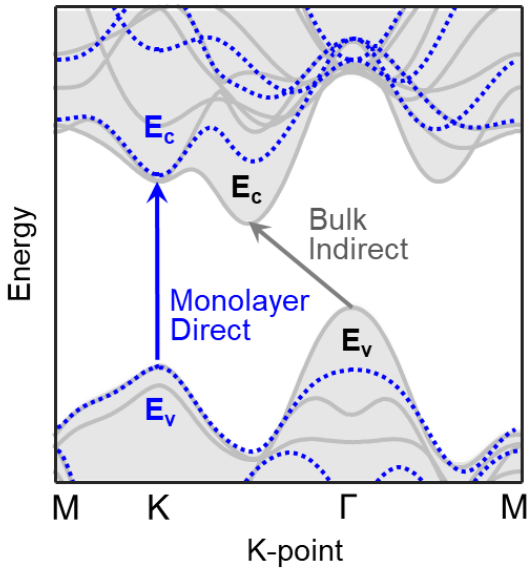


Figure 10: Typical band structure of semiconducting TMDs.

Among the TMD family, four types of monolayer TMDs- MoS_2, $MoSe_2$, WS_2, and WSe_2, have received most attention due to the abundance of corresponding bulk materials. The carrier effective masses (0.3 – 0.7 m_0, where m_0 is the electron mass) of them are generally larger than commonly used semiconductors, such as Si, Ge and III-V. Although dangling bonds are absent in monolayer or few-layer TMDs, scattering mechanisms, such as phonon scattering, Coulomb scattering, and surface roughness scattering degrade the carrier transport. Theoretical calculations have predicted that the maximum electron mobility at room temperature for n-type MoS_2 is only ~410 $cm^2\ V^{-1}\ s^{-1}$, primarily owing to optical phonon scattering **[95]**.

C. Common Properties

1. Layered Structure, Ultra-small and Uniform Thickness

2D materials consist of vertically stacked layers held together by relatively weak van der Waals force and each layer is formed of covalently bonded atoms. Hence, they are also called “van der Waals (vdW) crystals”. The thickness of each layer is only a few Ås, as shown in **Table 3**. The weak inter-layer bonding allows them to be mechanically exfoliated from bulk to form atomically thin flakes, for example, graphene can be exfoliated from bulk graphite.

Moreover, thickness of 2D material is determined by the number of layers, and hence, is discrete. Therefore, the thickness is more uniform compared to 3D bulk materials, as illustrated in **Figure 11**, which minimized the surface roughness.

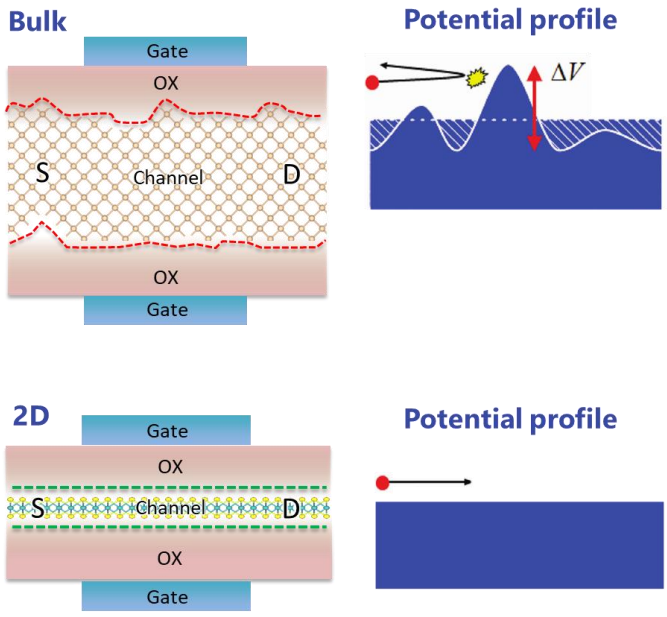


Figure 11: Advantage of uniform 2D film thickness – no surface roughness.

Table 3: Monolayer (1L) thickness of representative 2D materials.

Material Name	For-mula	1L thickness (nm)	Material Name	For-mula	1L thickness (nm)
Graphene	C	0.34	Rhenium Disulfide	ReS_2	0.64
Silicene	Si	0.44-0.46	Chromium Disulfide	CrS_2	~ 0.65
Germanene	Ge	~ 0.5	Germanium Disulfide	GeS_2	~ 0.65
Stanene	Sn	~ 0.5	Hafnium Disulfide	HfS_2	~ 0.65
2d Lead	Pb	~ 0.5	Molybdenum Diselenide	$MoSe_2$	~0.8
2D Silicon Carbide	SiC	0.5	Tungsten Diselenide	WSe_2	0.7
Siligene	SiGe	~ 0.5	Tin Diselenide	$SnSe_2$	0.65
2D Boron Nitride	BN	0.34	Rhenium Diselenide	$ReSe_2$	0.656
2D Phosphorus Nitride	PN	0.4343	Chromium Diselenide	$CrSe_2$	~ 0.7
Germanane	GeH	0.53	Hafnium Diselenide	$HfSe_2$	~ 0.7
Stanane	SnH	0.441	Molybdenum Ditelluride	$MoTe_2$	~ 0.7
Molybdenum Dioxide	MoO_2	~ 0.5-0.6	Tungsten Ditelluride	WTe_2	0.699
Tungsten Dioxide	WO_2	~ 0.5-0.6	Gallium Sulfide	GaS	~0.8
Chromium Dioxide	CrO_2	~ 0.5-0.6	Gallium Selenide	GaSe	0.93
Germanium Dioxide	GeO_2	~ 0.5-0.6	Indium Sulfide	InS	~ 0.8
Scandium Dioxide	ScO_2	~ 0.5-0.6	Indium Selenide	InSe	0.83
Manganese Dioxide	MnO_2	~ 0.5-0.6	Phosphorene	P	0.5
Nickel Dioxide	NiO_2	~ 0.5-0.6	Germanium Selenide	GeSe	0.54
Vanadium Dioxide	VO_2	~ 0.5-0.6	Tin Monosulfide	SnS	0.57
Molybdenum Disulfide	MoS_2	0.6-0.7	Tin Monoselenide	SnSe	0.575
Tungsten Disulfide	WS_2	0.62	Borane	B	0.7-0.8
Tin Disulfide	SnS_2	0.589	Titanium Trisulfide	TiS_3	0.89

2. Pristine Surfaces/Interfaces

The atoms in each layer of 2D materials, are all saturated and typically no more covalent bonds can be formed. Hence, the surfaces are pristine and there are no dangling bonds, as illustrated in **Figure 12**. Such pristine surfaces can reduce trap density, NBTI and flicker noise **[149]**.

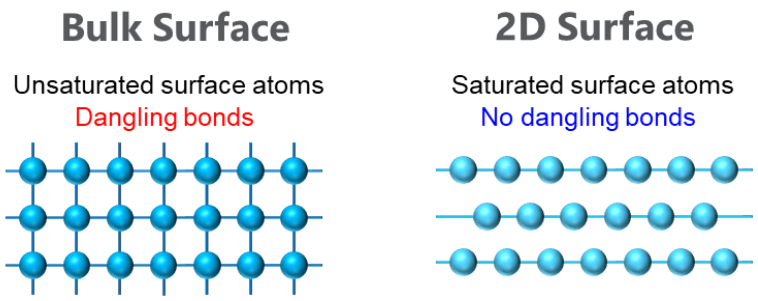


Figure 12: Pristine surfaces of 2D materials compared to bulk materials.

Moreover, due to the pristine surfaces, stacking different 2D materials on top of each other will form van de Waals (vdW) interface, as shown in **Figure 13**. Due to the much weaker interaction of vdW force, strain-free stacking of 2D materials is possible, without worry of the lattice mismatch issue.

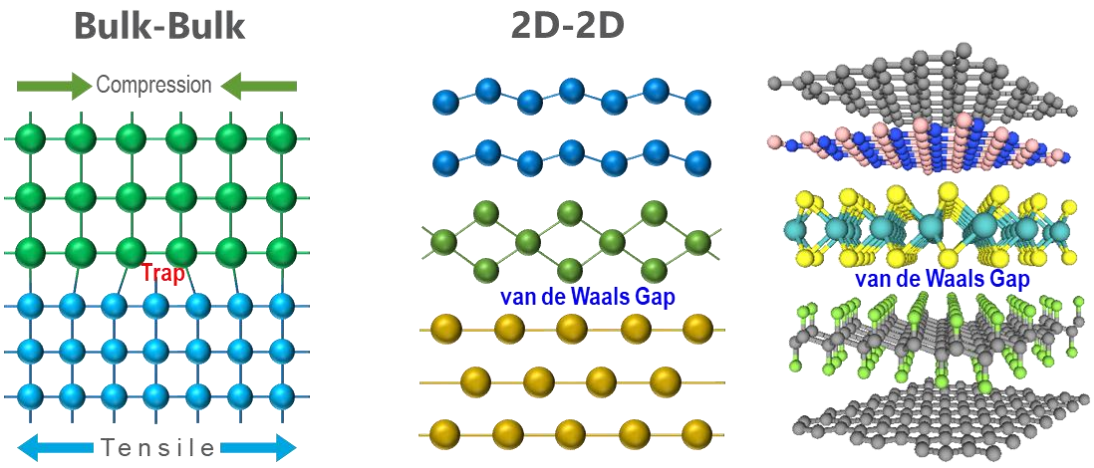


Figure 13: Advantage of van der Waals interfaces – no lattice mismatch or strain.

D. Band Gaps, Effective Masses and Mobilities

The search for 2D atomic layers that covers the entire spectrum of electronic properties has yielded a rich set of materials genome; from wide bandgap (>5 eV) insulator (hexagonal

boron nitride; h-BN) to semiconductors with bandgaps ranging from 0.5-3 eV (e.g., a variety of TMDs), there has been a flurry of activity to identify and create these 2D atomic layers with varying electronic properties.

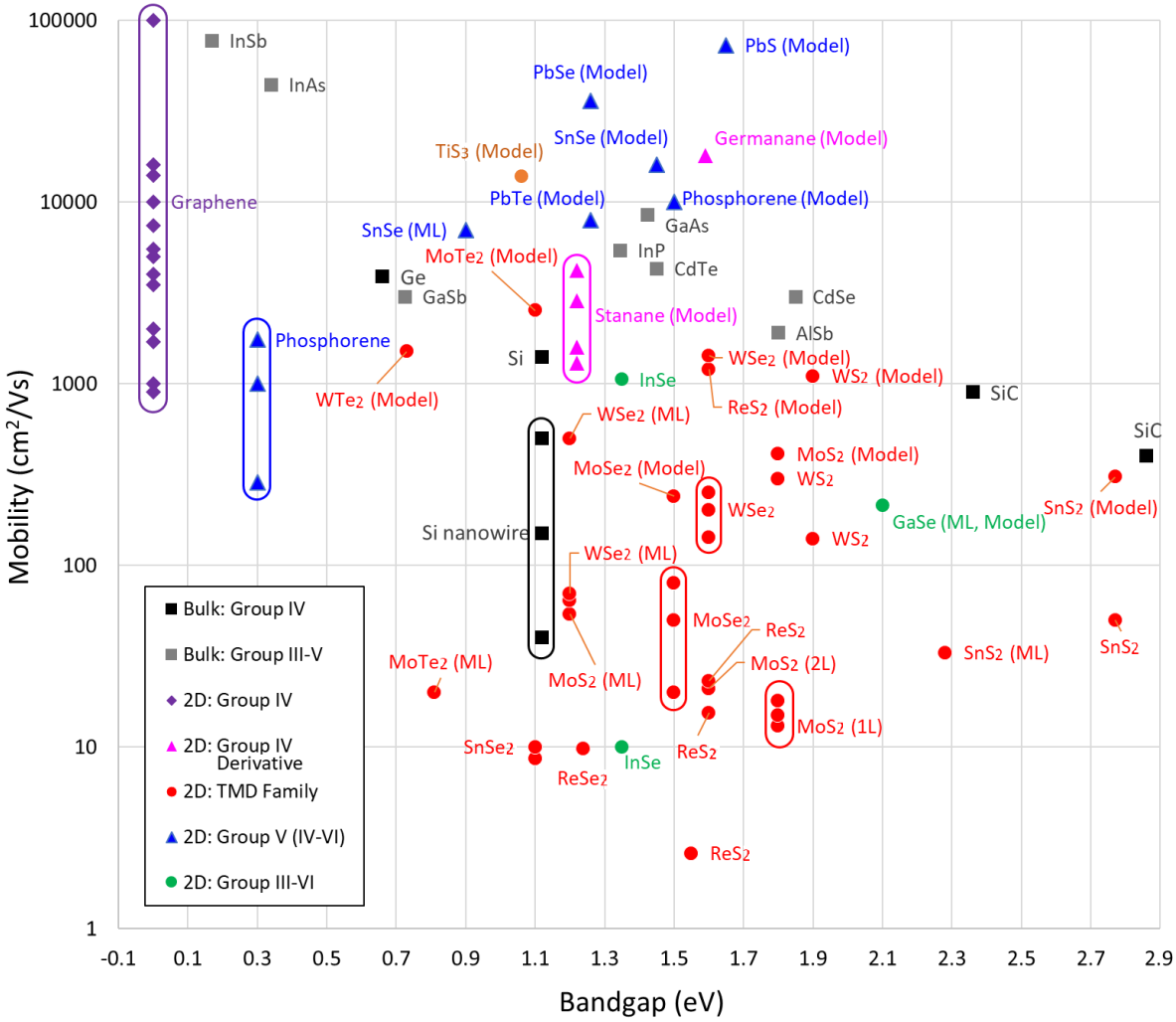


Figure 14: Mobility and bandgap of various 2D materials.

2D materials from the 5 main groups (IV, IV-Derivative, TMD, V, and III-VI) are compared with conventional bulk materials. "Model" indicates theoretically predicted mobility/bandgap. 1L stands for monolayer, while ML represents multilayer.

Here, the basic material properties – band gap, mobility and effective mass of tens of representative 2D materials (especially 2D semiconductors) are summarized in a few benchmarking plots, in **Figure 14**, **Figure 15**, **Figure 16** and **Figure 17**.

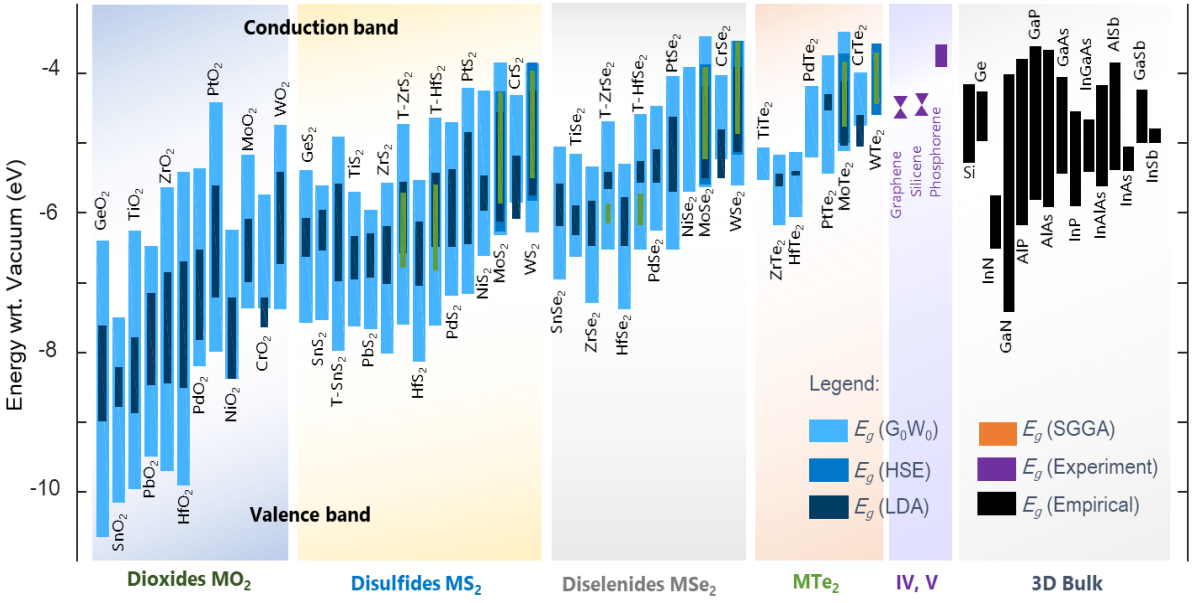


Figure 15: Band alignments of representative 2D and 3D materials.

G0W0, HSE, LDA, and SGGA are different calculation methodologies (exchange-correlation functionals for ab-initio simulations).

The extremely high carrier mobilities (up to 10^6 cm^2/Vs, as shown in **Table 4**) of graphene is one of the most attractive properties for the field of electronics research. However, the carrier mobility in graphene devices is usually much lower than expectation because of various scattering mechanisms at the interfaces between underlying/overlying dielectrics and graphene. Two major scatterers are surface phonons and ionized impurities **[150]**. In 3D materials, these issues cause less problem than in graphene, where there is only a single atomic layer. Even though the use of high-*k* dielectric helps screen the Coulomb

scattering due to impurities, the surface phonon scattering caused by the high-*k* material comes to dominate the mobility, according to theoretical calculations **[151], [152]**.

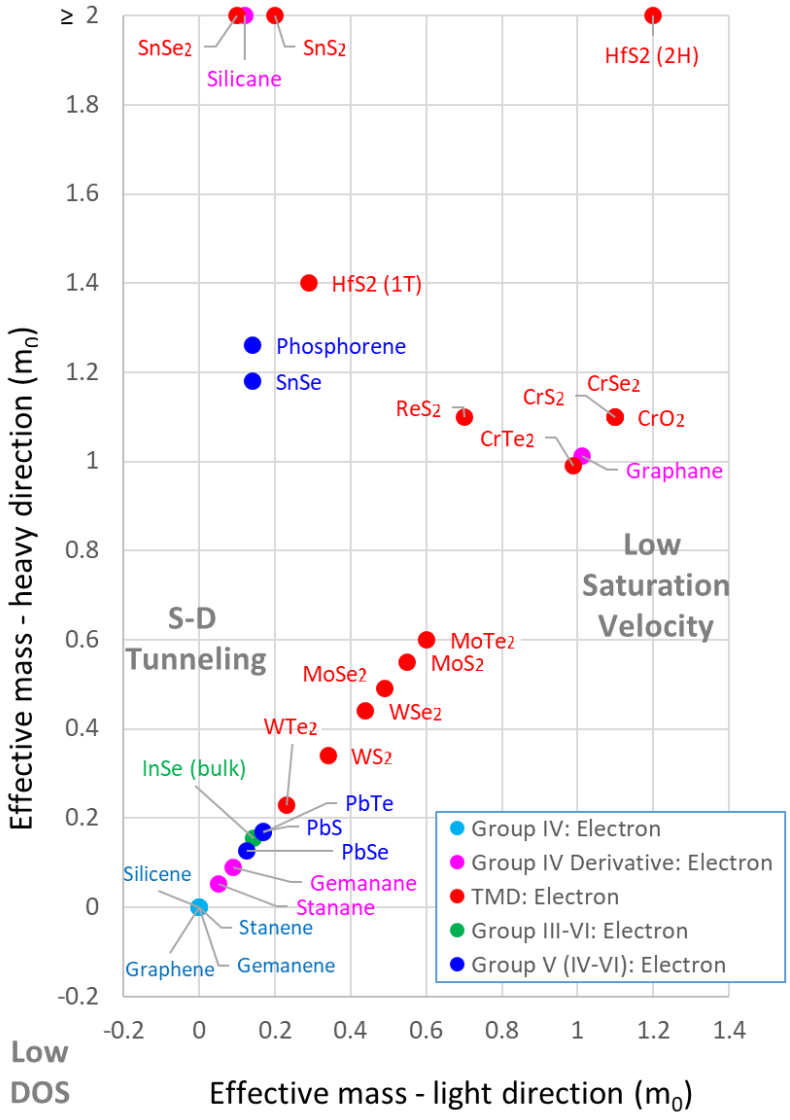


Figure 16: Electron effective masses of representative 2D materials.

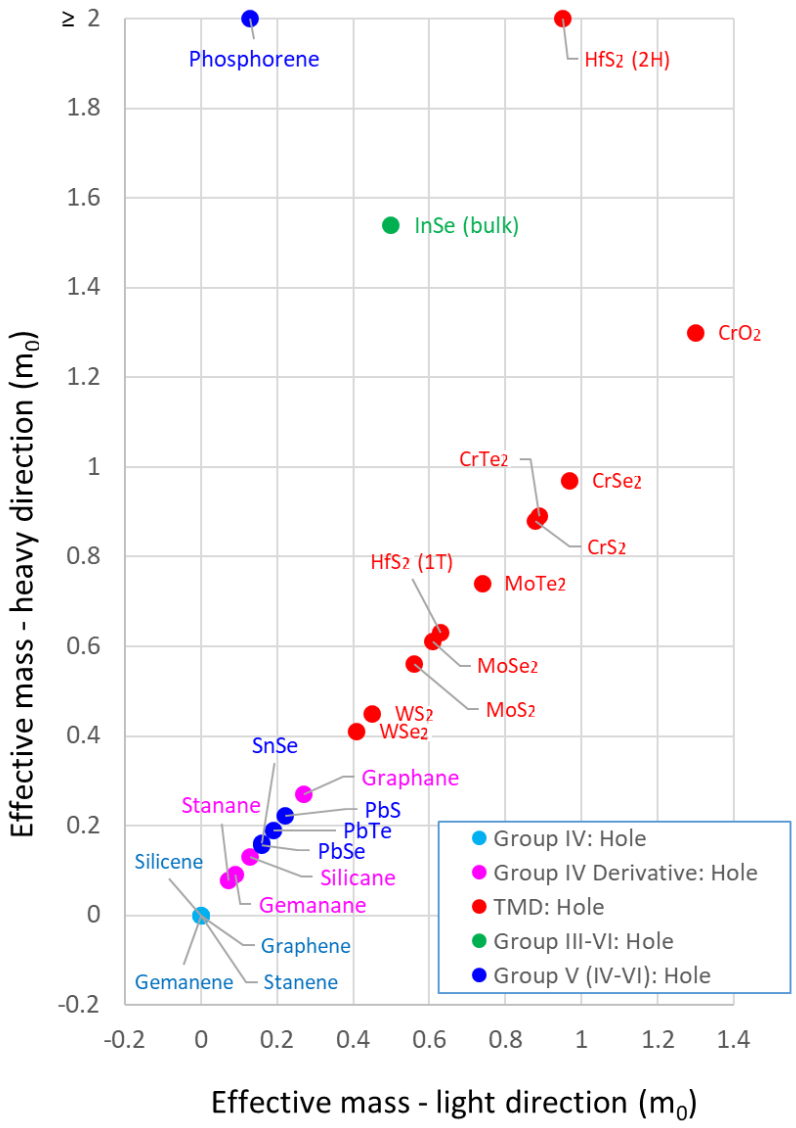


Figure 17: Hole effective masses of representative 2D materials.

E. Preparation of 2D Materials

1. Synthesis of Graphene

The simplest and cheapest method to prepare monolayer, bilayer, or few-layer graphene, so far, is the micromechanical exfoliation technique **[88], [153]–[155]**, which was found to provide sufficiently high-quality graphene, confirmed by the observation of room

temperature quantum Hall effect **[147]**. The reason is that Quantum Hall effect can only be observed in high mobility materials with high purity. However, mechanical exfoliation of graphite is only applicable for small-size graphene production for academic use, which makes it less efficient, not scalable and not controllable for industry-level production.

Table 4: Mobility values obtained in graphene by different growth methods. Results are shown for different numbers of layers and various synthesis methods.

Method	Condition	# of layers	Mobility (cm^2/Vs)	Ref.
Exfoliation	SiO_2 substrate	1	10000	**[88]**
	SiO_2 substrate	2	1000	**[136]**
	SiO_2 substrate	2	1700	**[139]**
	SiO_2 substrate	3	900	**[139]**
	Al_2O_3 substrate	1	7400	**[153]**
	h-BN substrate	1	14000	**[154]**
	Suspended	1	100000	**[155]**
Sublimation	SiC substrate	1-few	5000	**[156]**
Reduction	Graphene oxide	1	1000	**[157]**
CVD	Ni catalyst	1	5000	**[158]**
		1-few	2000	**[159]**
	Cu catalyst	1	16000	**[160]**
		1	7350	**[161]**
		1	4000	**[162], [163]**
		2	5500	**[164]**
	Ni+Cu catalyst	2	3500	**[165]**

So far, beside micromechanical exfoliation, several other methods have been successfully developed, such as sublimation (thermal graphitization) of SiC **[156], [166],**

[167] (**Figure 18a**), reduction of graphene oxide **[157]**, and epitaxial growth on metal substrate by catalyst-assisted chemical vapor deposition (CVD) **[158]–[165], [168], [169]**. Although sublimation of SiC is a wafer-scale method, the synthesized graphene cannot be transferred to other substrates.

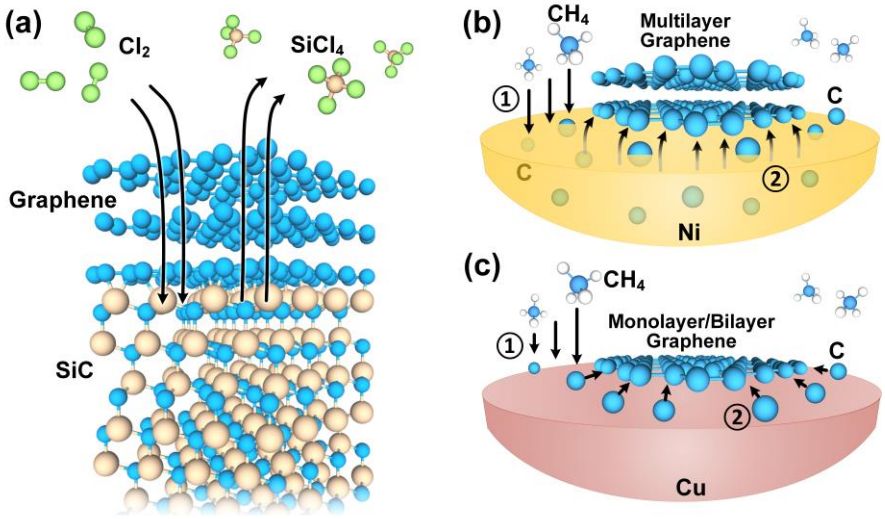


Figure 18: Graphene Synthesis Mechanisms.

(a) sublimation of SiC (decomposition of SiC in Cl_2 into graphene and $SiCl_4$); (b) CVD on Ni (1: dissolution of C into Ni, and 2: precipitation of multilayer graphene upon cooling); (c) CVD on Cu (1: nucleation of C, and 2: surface catalytic growth of monolayer/bilayer graphene).

On the other hand, CVD method, which uses single crystalline transition metals such as Cu or Ni as catalyst, has been proposed as a promising approach with higher efficiency and scalability. Graphene grows on Ni surface through a carbon dissolution-precipitation process (**Figure 18b**), using the carbon solubility in Ni at high temperature **[159], [168], [169]**. However, carbon has different precipitation behavior on the surface grain boundaries of Ni

film, hence resulting in non-uniformity of the synthesized graphene.

Compared with Ni, Cu has a better capability to grow high quality and uniform graphene. Graphene growth on Cu mainly depends on a surface catalytic process due to the nearly zero carbon solubility below Cu's melting point (**Figure 18c**). Many efforts have been spent to explore the growth mechanism of graphene to improve the quality of graphene and was found that graphene growth on copper is influenced by many factors, such as temperature, impurity of copper, partial pressure of carbon source **[164], [170]**. Through tuning these parameters, high quality and uniform graphene can be achieved. To date, 30-inch graphene film has been demonstrated by a roll-to-roll method **[161]**, indicating the possibility to produce graphene films in industrial scale.

Recently, direct graphene growth on dielectric substrates by CVD has also been developed **[171]–[174]**. In these processes sacrificial metal catalyst layers are directly prepared on dielectric substrates and are removed after graphene growth by various etching techniques (dissolution by Marble's reagent **[172]**, Cl_2 dry etching **[173]**, etc.), affording graphene directly on the substrate.

For fabrication of GNRs, lithographic patterning (normally using electron beam lithography for high resolution) of graphene **[142]** is the most natural choice (which is categorized as a "top-down" method), although edge roughness remains a challenge. Other synthesis methods include chemical synthesis **[141], [175], [176]**, selective epitaxial growth **[177]**, unzipping of carbon nanotubes **[178], [179]**, etc. (categorized as a "bottom-up" method), in which the controllability of ribbon width, position, edge quality, and yield are still under improvement.

2. Synthesis of Other 2D Materials

Due to the similar layered structure of bulk TMD materials as in graphite, synthesis of

monolayer TMDs has been sharing the experience gained in graphene synthesis. Two primary methods are exfoliation (mechanical/chemical), and chemical vapor deposition (CVD) growth. CVD growth has been proved to be the most reliable way to grow large area (up to wafer scale) MoS_2 films. In general, CVD method includes sulfurization of MoO_3 **[180]–[182]**, MoO_2 **[183]**, or Mo layers pre-deposited on substrates **[184]**, or thermolysis of Mo compound $(NH_4)_2MoS_4$ on substrates **[185]**. The thermolysis of $(NH_4)_2MoS_4$ is the first method that produced large scale MoS_2 film. However, this method has a complex process including precursor preparation and post annealing to enhance the quality of MoS_2 film. Using solid phase sulphurization of MoO_3, $MoCl_5$ or Mo thin films method, large single crystal MoS_2 domain (>100μm), and large area MoS_2 films have been grown on SiO_2 substrates. In addition, the qualities of CVD synthesized MoS_2 are comparable to those of the exfoliated MoS_2 films within one domain. The synthesized large area MoS_2 film has large amount of grain boundaries, which can markedly influence the electrical property of MoS_2 film. Hence, reducing grain boundaries in CVD MoS_2 film will significantly benefit MoS_2 electronic devices.

3. Transfer of 2D Materials

The high temperatures and long process time of most of the thermal approaches are not acceptable for the thermal budget limit of VLSI processes, especially in 2.5D/3D technologies. Therefore, to separate the growth step from other process steps, it becomes expedient to employ a wet transfer process (**Figure 19**)

The pros of this method are mainly the thermal budget (room temperature process) and preservation of crystal quality. The wet transfer, however, is not a scalable or CMOS compatible method that can be used in an industrial setup. Moreover, the cost of such method is high due to the fact that the growth substrate has to be dissolved and thus both the

substrate and the solution are wasted.

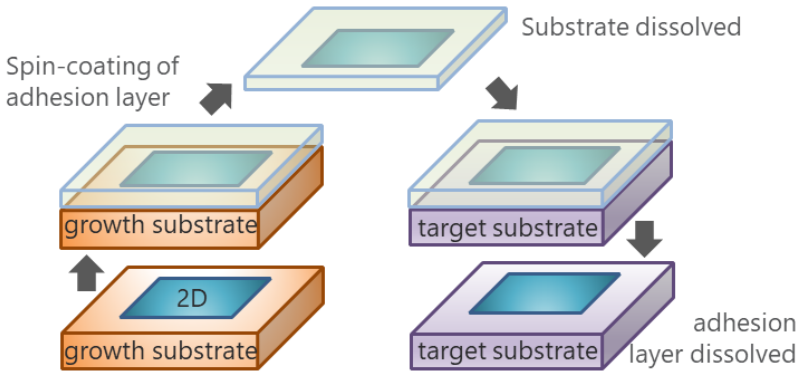


Figure 19: Wet transfer process of 2D materials.

Direct growth on target substrate at low temperature in short time is always desired for raising the technology readiness level of 2D technologies. Challenges of such method include selective catalyst issue, thermal budget issue and interface issue. The interface issue includes both the impurities and the interface traps. The impurities mainly come from the residues of all the chemical methods (including various chemical vapor deposition (CVD) schemes, atomic layer deposition (ALD) and molecular beam epitaxy (MBE)), where more than one precursors are involved. The traps, as will be shown later in **Chapter IV** by density functional theory (DFT) simulations, are induced by the interface bonding during high temperature growth process.

4. Patterning of 2D Materials

Precise lithography technologies need to be developed to provide feasibility for the device applications of 2D materials. Etching of 2D materials is a case by case issue. For example, etching of graphene can be done by oxygen plasma, where the product is only CO_2. For MoS_2, a dry etching method based on XeF_2 gas can be employed **[186]** since all the

products are gas phase (Xe, $MoF_{2,3}$, F_2 and SF_6). This method (**Figure 20**) will be used frequently in this dissertation in the following chapters.

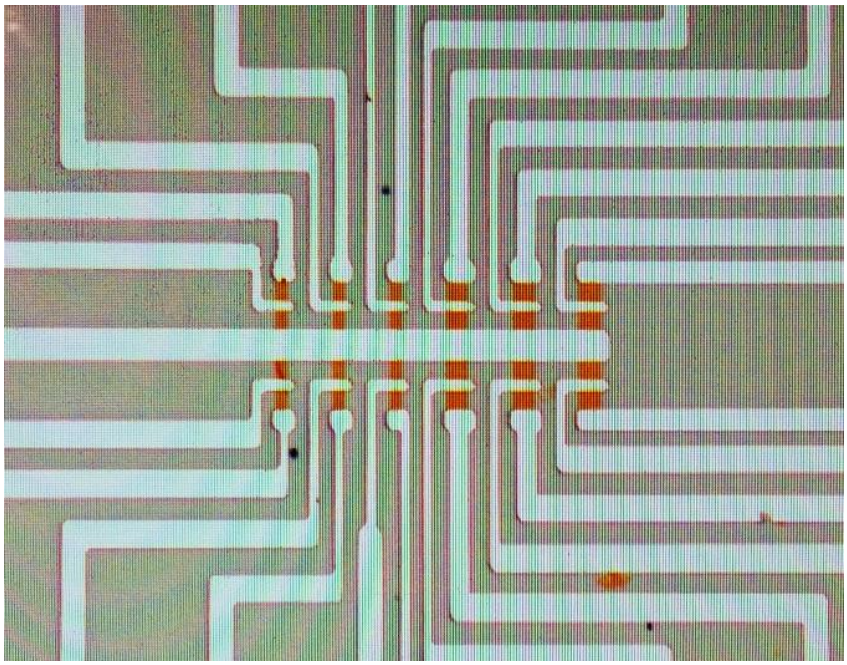


Figure 20: Array of MoS_2 transistors etched by XeF_2.

F. Stability of 2D Materials

The chemical and thermal stabilities of some typical 2D materials are summarized in **Figure 21**, **Figure 22** and **Figure 23**, based on the only available data from literature **[146], [187]–[192]**. It can be seen that the Group-IV derivatives are typically instable **[146], [187]–[189]**, so as group V (especially black phosphorus) **[193]–[201]**, while TMDs are relatively stable in both air and vacuum **[190]–[192]**.

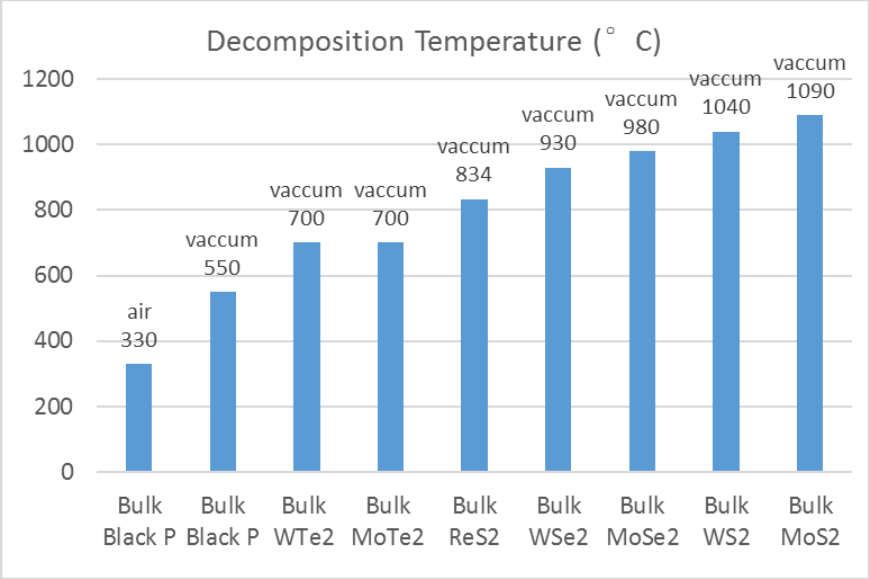


Figure 21: Stability of some bulk 2D materials in air and vacuum.

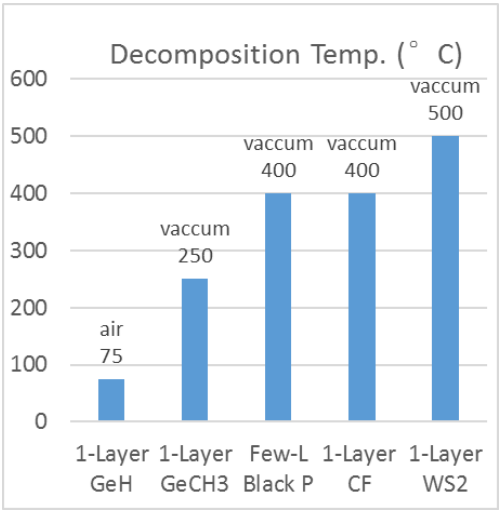


Figure 22: Stability of some 1L 2D materials in air and vacuum.

In addition, TMDs with lighter atom weights typically have better stability, as shown in **Figure 21**, but lower mobility (as shown in **Section D**). For black phosphorus, an encapsulation layer can help slow down the degradation of few layer **[196]–[201]**.

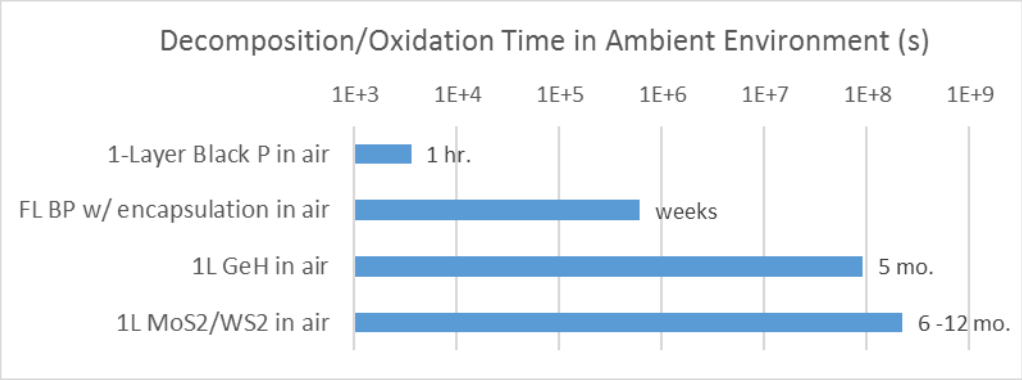


Figure 23: Stability of some 2D materials in ambient temperature.

G. Chapter Summary

The families of 2D crystal cover the entire spectrum of electronic properties, from wide bandgap (>5 eV) insulator (hexagonal boron nitride; h-BN) to semiconductors with bandgaps ranging from 0.5–3 eV (e.g., a variety of TMDs), and to metallic crystals including half metals (bandgap < 0.5 eV) and semimetals (with overlapped conduction and valence bands). There has been a flurry of activity to identify and create these 2D atomic layers with varying electronic properties. These unique and wide-ranged properties can be exploited to demonstrate completely different device technologies. The following chapters will present how these properties can be utilized in emerging applications by overcoming their integration challenges.

III. Metal Contacts to 2D Materials

A. Introduction

Electrical contacts to 2D layered crystals including graphene, semiconductors of the transition-metal dichalcogenide (TMD) family such as molybdenum disulphide (MoS_2) and tungsten diselenide (WSe_2), as well as other emerging 2D semiconductors such as atomically-thin black phosphorus, play a central role in determining the performance of electronic and optoelectronic devices and circuits made from them. This chapter presents a comprehensive study of the physics of such interfaces and discusses solutions toward realizing optimal contacts to these materials.

The typical value of metal-1L-TMD contact resistance is at least in the order of kΩ μm and is usually 1–3 decades higher than that of metal-silicon contacts in complementary metal oxide semiconductor technology (order of 0.1 kΩ μm) **[50]**. Such high contact resistances between metals and 1L-TMDs significantly degrade the performance of TMD transistors **[92]**. Since there is currently no stable and reliable doping method to lower the contact resistance, it is highly desirable to explore suitable metals and contact configurations, which have the maximum potential to form low-resistance metal-1L-TMD contacts. To find the optimal contact metals, several studies on specific cases of metal-TMD contacts have been reported recently: (1) Ti-MoS_2 and Au-MoS_2 top contacts **[202]** with top-contact configuration, which are only qualitatively studied by density-functional theory (DFT) in the absence of the treatment of van der Waals (vdW) interaction (which will be discussed later); (2) Sc, Ni, and Au contacts to multilayer MoS_2 **[91]**; (3) Ti contacts to multilayer MoS_2 **[5]**; (4) Pd-WSe_2 contact **[25]**; (5) In-, Al-, and Ag-WSe_2 contact **[7]**; and (6) 2D compound metal contacts to MoS_2 **[203]** studied by DFT. However, these works are

not systematic and lack the rigorousness necessary for accurate analysis.

Hence, it is necessary to develop a comprehensive understanding of the nature of the electronic interface between metals and 1L-TMDs, going beyond the analytical Schottky barrier (SB) theory. As mentioned above, currently such a comprehensive study of metal-1L-TMD contacts is still lacking. For example, diversity of metals, calculation of Schottky barrier height, and/or treatment of vdW force have not been considered simultaneously in all previous works. Moreover, all of the computational studies address only the properties of metal-1L-TMD top contacts (**Figure 24a**) **[202], [203]**, while the edge contacts (**Figure 24b**) have not been reported. Since 2D crystals are fundamentally different from 3D crystals in that the surface has no dangling bonds, one has to take advantage of the edges where there are dangling bonds for intimate chemical bonding for charge transfer.

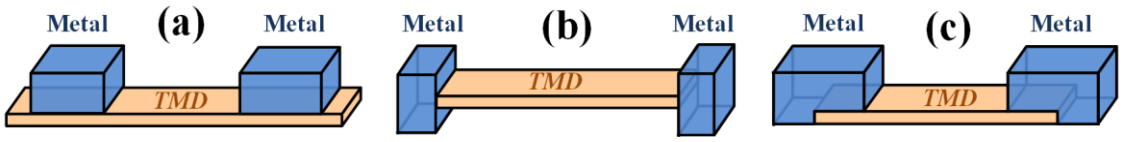


Figure 24: Schematic of metal-1L-TMD contact geometries.

(a) top contact, (b) edge contact, and (c) combined contact.

It is worth noting that in most experiments, the contacts to 2D materials are a combination of these two geometries (**Figure 24c**). pure top-contacts can be made on purpose **[204]**, by simply avoiding contact between the metal and the edges of the 2D material. The formation of a pure edge-contact using standard lithographic techniques is however difficult in a mono- or few-layer 2D material, due to the atomically thin body, and so far, only one example has been reported **[205]**, where a graphene monolayer was purely edge-contacted.

In this chapter, firstly I discuss the origins of the metal contact challenges. Then I present a systematic study of the contacts between 1L-TMDs (monolayer MoS_2 and WSe_2) and various metals (In, Ti, Au, Pd, Mo, and W) for different contact geometries (top and edge contacts) by DFT considering the effect of vdW force. With the novel quantitative computational methodology presented in this work, I highlight and illustrate how to estimate the orbital overlaps and the Schottky or tunnel barriers to atomistic accuracy. It is shown that apart from choosing a proper work-function (WF) metal, the detailed physics of the interface between the metal and the 1L-TMD layers plays an important role, which should be understood to achieve low contact resistances.

I then move on to discuss demonstrated contact resistance in my experiments, and present an overview of the current values reported in this area. Finally, I propose a novel technique to minimize contact resistance the "seamless contact". Because of the easy availability of MoS_2, WSe_2 and graphene, most of the research on devices based on 2D materials is currently being carried out using these materials. Concepts and limitations that we outline here can, however, be readily extended to other 2D semiconductors.

B. Origin of Contact Challenge

The quantum limit to the contact resistance ($R_C^{\min}$) is determined by the number of conducting modes within the semiconductor channel **[206], [207]**, which is connected to the 2D charge carrier density (n2D), yielding $R_C^{\min} = h/(2e^2 k_F) = 0.026/\sqrt{n_{2D}} \approx 30\ \Omega.\mu m$ at $n_{2D} = 10^{13}$ cm^{-2} **[208]**, a value three orders of magnitude below the typical contact resistance to monolayer MoS_2. Here, h is the Planck's constant, k_F is the Fermi wavevector and e is the electron charge. Thus, there is a lot of room for improvement and it is important to study the detailed physics of the contacts between metals and the 2D semiconductors.

1. The van der Waals Gap

Contrary to the case of bulk (3D) semiconductors, **Figure 25a** and **Figure 25b**, the pristine surfaces of 2D materials, do not tend to form covalent bonds. The interfaces between the metals and 2D materials in top-contacted configuration can thus only be formed by a van der Waals (vdW) gap in most situations, **Figure 26** and **Figure 25c**. As shown in **Figure 25d**, the vdW gap in such top-contact interfaces acts as an additional "tunnel barrier" for carriers, before the inherent Schottky barrier (SB) **[2]**. The tunnel barrier greatly reduces the charge injection from metals resulting in higher contact resistance.

As mentioned earlier, most practical contact structures involve both the edge and the top surface of the 2D material, with the top surface having a large contribution due to the large surface-to-perimeter ratio. Hence, the contact resistance can be improved by reducing the tunnel barrier at the top surface. This can be achieved by hybridization between atoms of contact metals and 2D semiconductor surfaces.

DFT simulations in later sections show that specified metals can form covalent bonds to 2D semiconductor surfaces (**Figure 25e**), and hence eliminate the vdW gap, for example, Ni for graphene **[209]**, Ti for MoS_2 **[1], [202]**, Pd for WSe_2 **[1]**, Mo/W for MoS_2/WSe_2 **[2], [6]** and Ti_2C (a 2D metallic material) for MoS_2 **[203]**.

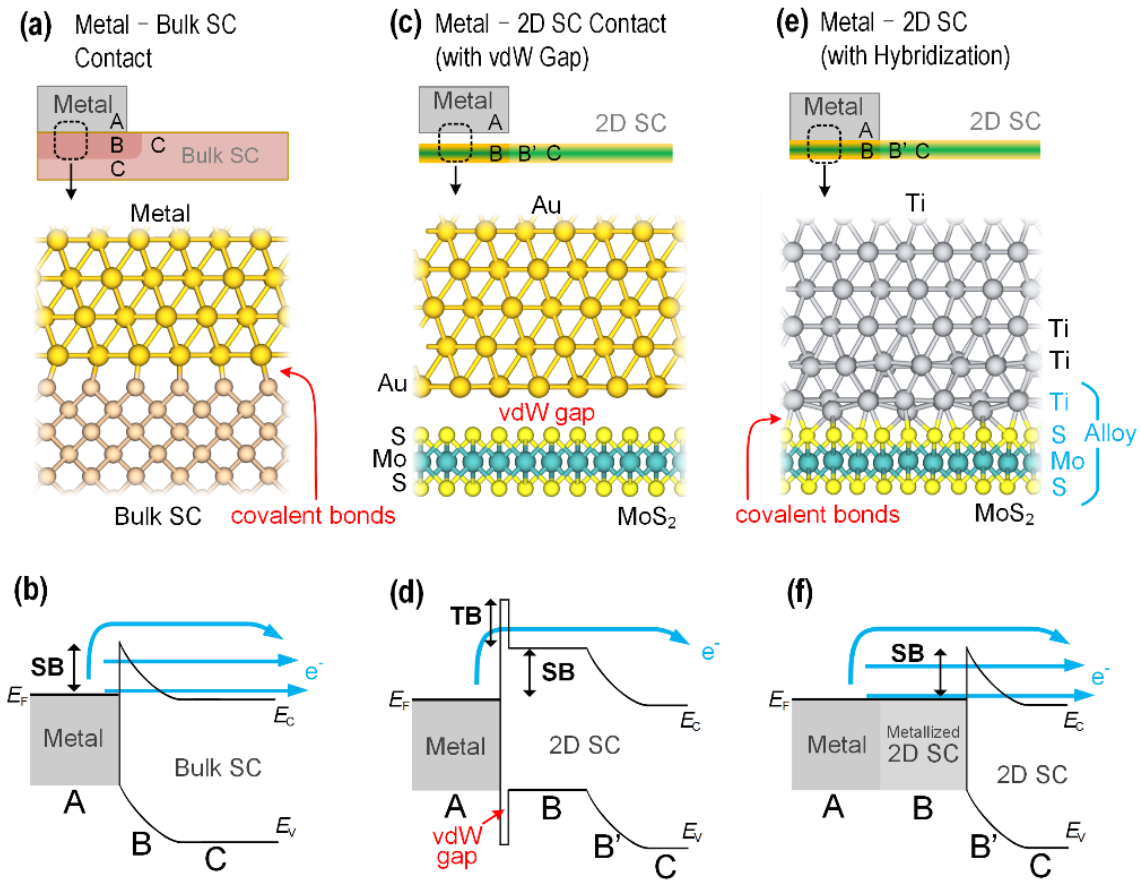


Figure 25. Types of metal-semiconductor junctions and their band diagrams.

(a, b) Schematic and band diagram of typical metal – bulk semiconductor (SC) interface; (c, d) metal - 2D SC interface with van der Waals (vdW) gap (example: Au-MoS_2 contact); (e, f) metal - 2D SC interface with hybridization (example: Ti-MoS_2 contact, where MoS_2 under contact is metallized by Ti). E_F, E_C and E_V represent Fermi level of metal, conduction and valence bands of 2D SC, respectively. TB and SB indicate the tunnel and Schottky barrier heights, respectively. A, B, B' and C represent different regions in the current path from the metal to the SC. The blue arrows in (b), (d) and (f) represent the different injection mechanisms. From top to bottom: thermionic emission, thermionic field emission and field emission (tunneling). In (d), only thermionic emission is available.

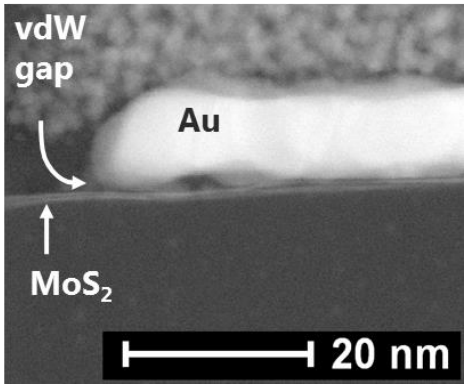


Figure 26: Transmission electron microscopy image of an Au-MoS_2 contact.

Strong hybridization, as will be shown later, can also distort the properties of 2D semiconductors below the top-contacts (especially for monolayer) **[6]**. This can result in a change of the sheet resistance of 2D semiconductors below the contacts ($\rho_{contact}^{2D}$), and thus in a change of contact resistance (the calculation of which will be discussed in a later section). It should be noted that $\rho_{contact}^{2D}$ can be either increased or decreased by hybridization. DFT predicts that selected metals such as Ti and Mo create non-localized overlap states in the original band gap of MoS_2 **[2]**, effectively turning MoS_2 under the contact into a new metallic compound (**Figure 25f**). In such situation, $\rho_{contact}^{2D}$ reduces. On the other hand, if the monolayer is partially metallized, $\rho_{contact}^{2D}$ may increase due to localized states.

2. Dimensionality and Current Crowding

Contrary to the bulk case (**Figure 25a,b**), where the diffusion region B extends both laterally and into the depth of the semiconductor, in metal/2D-SC junctions with no hybridization (**Figure 25c,d**), the position of the bands only vary laterally, and charge carriers injected far from the contact edge first encounter a region of flat band B before the

diffusion region B'**[2]**, **Figure 25c,d**. In this case, the relative contributions from thermionic emission and tunneling become hard to predict. Here in this part, the transmission line model will be used to analyze such phenomena and the outcome of it.

The most common contact geometry in use today is the top-contact. In the weak coupling limit, the contact resistance is a combination of the resistivity r_c of the metal/semiconductor interface (expressed in $\Omega \cdot m^2$) and of the semiconductor's sheet resistivity ρ^{2D} (expressed in Ω per square or Ω /□)**[210]**. If the contact is diffusive, that is if the charge carriers are scattered many times within the semiconductor before being kicked out of the semiconductor and into the metal, then the interface can be modeled as a resistor network, **Figure 27**. This is the so-called transmission line model **[211], [212]** (TLM), which gives the following expression for the contact resistance R_c in $\Omega \cdot m$:

$$R_C = \sqrt{\rho^{2D} r_C}\,\coth\left(l\sqrt{\frac{\rho^{2D}}{r_C}}\right) \tag{3}$$

where l is the contact length. It can be seen that the dependence of R_c on l is not linear because of current crowding. For contact lengths much larger than the transfer length $L_T = \sqrt{r_c/\rho^{2D}}$ (L_T is the average distance that an electron (or hole) travels in the semiconductor beneath the contact before it enters the contact), the expression for the contact resistance becomes $R_C = \sqrt{\rho^{2D} r_C}$ (in $\Omega \cdot m$) and is no longer dependent on the contact length. In some reports the "as-measured" resistance is referred to as the "contact resistance", in which case it is the contact resistivity which is expressed in units of $\Omega \cdot m$. The quantity "resistance × contact area" (in $\Omega \cdot m^2$) is sometimes also used to characterize contacts, especially when contacts exhibit a significant dependence on contact length l**[213]** (when l and L_T are of the same order).

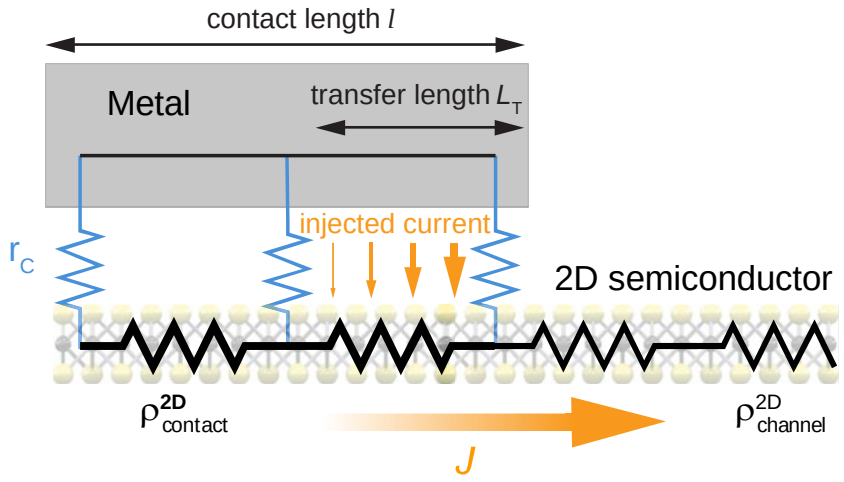


Figure 27. Current crowding at the contact edge region.

The resistor network illustrates the transmission line model. The orange arrows depict the current density. r_c represents the resistivity of the metal/semiconductor interface. $\rho^{2D}_{contact}$ and $\rho^{2D}_{channel}$ represent the semiconductor's sheet resistivity under the contact and in the channel, respectively.

In graphene, the diffusive approximation breaks down due to the longer electron mean free path (MFP), which calls for a ballistic treatment of the contact resistance**[214]**. In TMDs however, the much lower MFP implies that the TLM can be applied, provided that the resistivity of the portion of semiconducting material under the contact ($\rho^{2D}_{contact}$), and not the resistivity of the semiconducting channel ($\rho^{2D}_{channel}$), is used in place of ρ^{2D} in Equation 3. Note however that it cannot model the metal contacts to multilayers accurately due to the greater impact of edge contacts **[215]**,**[216]**.

The transfer length has been studied in monolayer **[217]** and 2L-6L **[218]** MoS_2. A value of L_T = 600 nm was found**[217]** in monolayer, assuming $\rho^{2D}_{contact} = \rho^{2D}_{channel}$. Using a more

elaborate measurement **[218]** similar to a four-terminal Kelvin resistor scheme described in**[210]**, one can accurately determine both $\rho_{contact}^{2D}$ and r_c. A value of $L_T = 20-70$ nm was thus found for bilayer MoS_2 with Ti contacts and up to 200 nm in 6L MoS_2**[218]**. This discrepancy indicates that the assumption $\rho_{contact}^{2D} = \rho_{channel}^{2D}$ fails in the case of atomically thin channels. This is due to the dramatic influence of the metallic electrode on the channel underneath them.

3D	2D
Contact length l < Transfer length l_T	Contact length l > Transfer length l_T
"As-measured" resistance (in unit of Ω) $R \propto w^{-1}l^{-1}$	"As-measured" resistance (in unit of Ω) $R \propto w^{-1}$
Contact resistivity R_c (in unit of Ωm²)	Contact resistance R_c (in unit of Ωm)

$$R_C = \sqrt{\rho^{2D} r_C}\coth\left(l\sqrt{\frac{\rho^{2D}}{r_C}}\right) \longrightarrow R_C = \sqrt{\rho^{2D} r_C}$$

Figure 28: Comparison of Metrologies for 3D and 2D Contacts.

3. Charge Injection Mechanisms

The two mechanisms through which charges can be injected into a semiconductor (SC) are thermionic emission over, and field emission (tunneling) across, the Schottky barrier (see **Figure 29**). The thermionic-emission-diffusion theory **[219]** describes the current-voltage characteristics of a metal/SC junction as a function of SBH. Carrier recombination can also be a limiting process if an inversion layer is present near the contact. This is mostly

the case in low-bandgap semiconductors (easy to form inversion layer) such as Ge nanowires**[220]** and could be significant in black phosphorus (small band gap Δ = 0.3 eV).

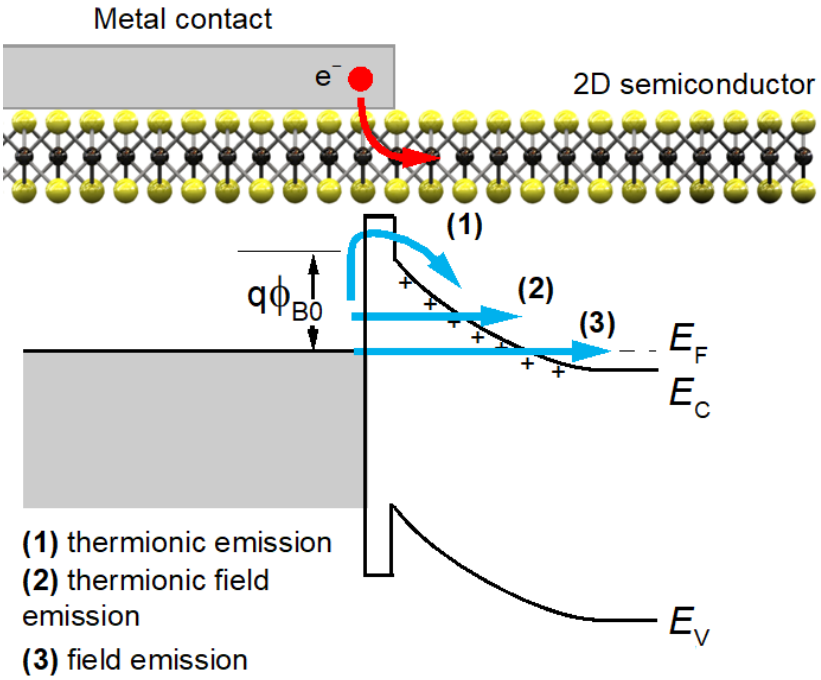


Figure 29. Charge injection mechanisms and extraction of Schottky barrier. The case with vdW gap (or without strong hybridization) is considered.

In TMDs, we should deal mostly with thermionic emission at low doping, with thermionic field emission starting to contribute as doping increases (**Figure 29a**), similar to the case of small geometry silicide contacts in advanced CMOS technologies**[221]**.

The charge injection into 2D semiconductors strongly depends on the SBH, and knowing its value and ways to alter it would allow optimization. In the ideal case, the SBH ϕ_{B0} between a metal and a semiconductor is determined by the difference $\phi_{B0} = \phi_m - \chi$ between the metal's work function ϕ_m and the semiconductor's electron affinity χ, also referred to as

the Schottky-Mott rule **[219]**. In reality however, the Fermi level at the metal/semiconductor interface is often pinned. We can quantify this by inspecting the SBH dependence on ϕ_m, quantified by $S = d\phi_{B0}/d\phi_m$, with $S = 1$ corresponding to the ideal case or Schottky limit, and $S \approx 0$ to that of a pinned Fermi level. The origin of this pinning in metal-bulk semiconductor interfaces is the presence of metal-induced gap states (MIGS)**[222]**. For metal contacts to 2D semiconductors, as will be discussed in later sections, the presence of a metal-MoS_2 alloy with a different work function **[2]** and the creation of gap states from the weakened intralayer S-Mo bonding **[223]** contribute to the pinning. The resulting reduced tunability of the SBH makes engineering of ohmic contacts by the choice of the contact metal (or work function) alone, less effective.

C. Top Contacts on 1L-TMDs – Computational Study

A computational study of metal-1L-TMD contacts is developed in four steps from the modeling and simulation framework, as listed in **Figure 30**: (a) choosing metals, (b) interface modeling, (c) DFT calculations (Sec. II C), and (d) contact evaluation (Sec. III).

In particular, the methodology includes van der Waals interactions and employs the bond Mulliken population analysis of interfaces between MoS_2 or WSe_2 and various metal contacts, which is more robust, visual, and insightful and can guide experimental work. Moreover, band structure calculations are used to extract the Schottky barriers between metals and MoS_2 or WSe_2.

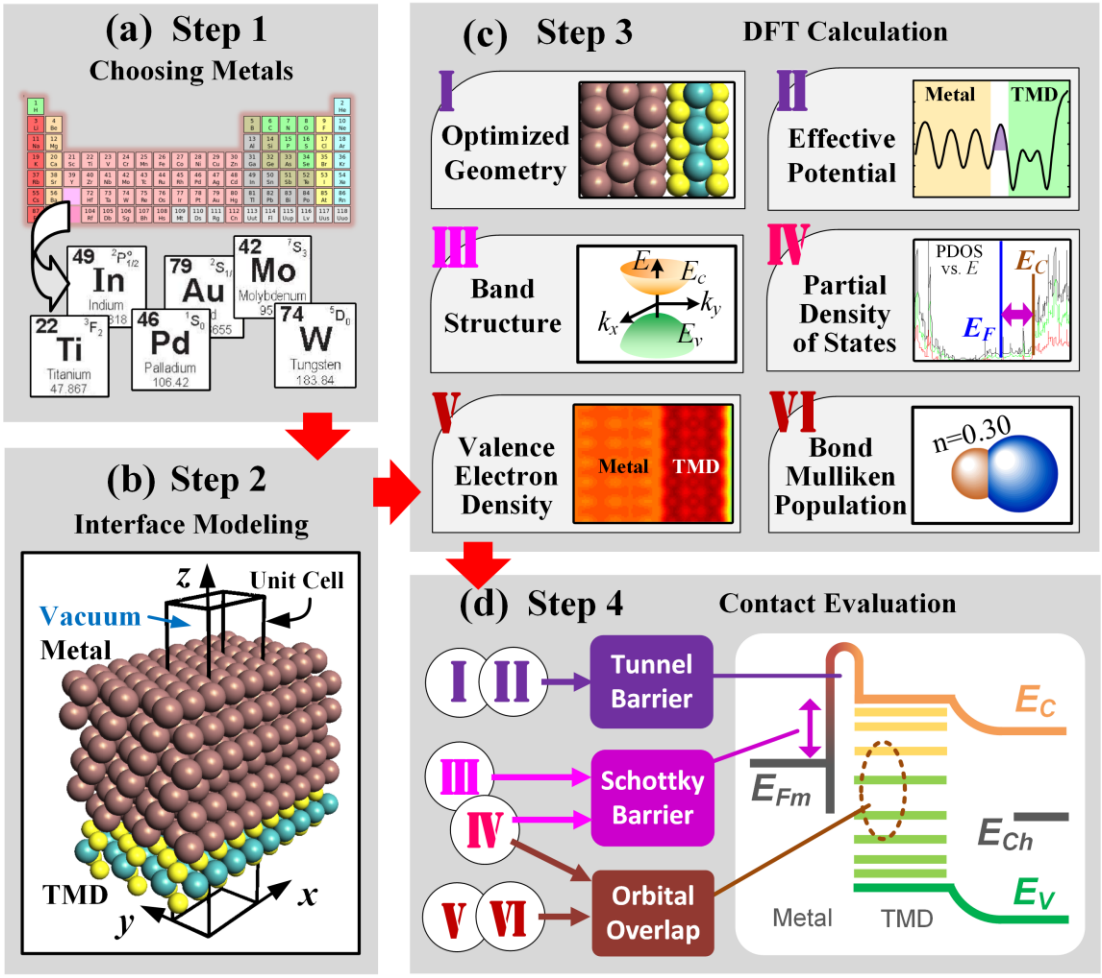


Figure 30: Framework for metal-1L-TMD contact computational study.

There are four steps: (a) choosing metals, (b) interface modeling, (c) DFT calculations, and (d) contact evaluation. E_{vac}, E_c, E_v, and E_F represent vacuum level, conduction band edge, valence band edge, and Fermi level, respectively. E_{Fm} and E_{ch} represent metal Fermi level and channel potential, respectively.

1. Choosing Metals

In terms of the process robustness and electrical reliability, the bulk contact metals are still the main strategy for 1L-TMDs compared to the 2D compound metals reported by Gan

et al. **[203]**. Considering fundamental physical properties (melting point and electrical and thermal conductances) as well as chemical properties (stability and toxicity) of all metals, Al, Ti, Cr, Ni, Cu, Pd, Ag, In, Pt, and Au are usually suitable as contact metals. However, the contact metals for 1L-TMDs should have either low WF to achieve small n-type SBs or high WF to achieve small p-type SBs. Cr can be excluded because of its unsuitable WFs with respect to the 1L-TMDs **[224]**. Furthermore, Cr and Ni can also be excluded due to the large lattice mismatches (percentage of lattice constant mismatch **[225]**) with 1L-TMDs, because small lattice mismatches are favorable, which can maximize orbital overlaps (**Figure 31**) **[202]**. Al is not a good contact metal for 1L-TMDs because of the absence of d orbitals, which can mix with the band-edge d orbitals of Mo and W resulting in the better electron injection (Fig. 6) **[7]**. In addition, our experimental results show that Al and Ni form high-resistance contacts with 1L-TMD **[7]**.

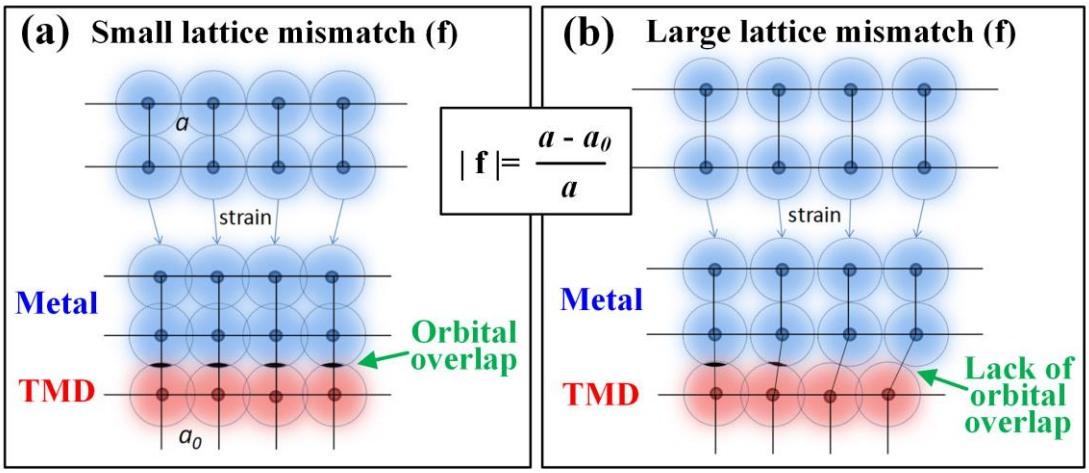


Figure 31: Schematics showing the impact of lattice mismatches.

(a) Small lattice mismatch that maximizes the orbital overlaps between metal and TMD. (b) Large lattice mismatch that prevents maximizing the orbital overlaps.

Based on the above criteria, In, Ti, Au, and Pd are first chosen as the contact metals for this study in both top- and edge-contact configurations. Although Mo and W have neither high nor low WFs (**Figure 32**) (Mo: 4.5 eV; W: 4.6 eV) **[224]**, they are the elements forming MoS_2 and WSe_2, respectively. Hence, Mo and W have great potential to form strong orbital overlaps with MoS2 and WSe2 by forming interface Mo-S and W-Se bonds. Therefore, Mo and W are included in this study as well.

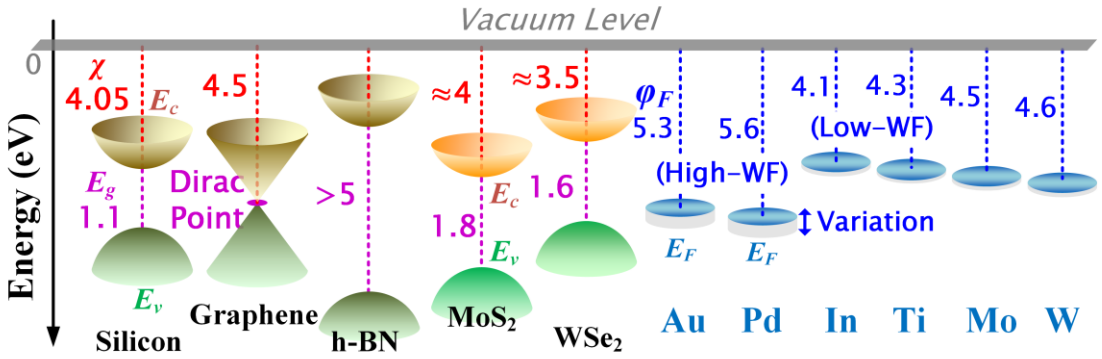


Figure 32: Band alignment of silicon, selected 2D materials, and contact metals.

***E_c*, *E_v*, and *E_g* represent conduction band edge, valence band edge, and band gap, respectively. χ and ϕ_F represent electron affinities and metal work functions (WFs), respectively.**

It is important to note that WF alone is not sufficient to form good contacts, as will be revealed in the subsequent sections in this paper. In Schottky theory, only an extremely high-WF or low-WF metal can form an Ohmic contact when Fermi level pinning is absent. However, in the absence of efficient doping methods for 1L-TMDs, nearly no metal has such a high or low WF with respect to 1L-TMDs.

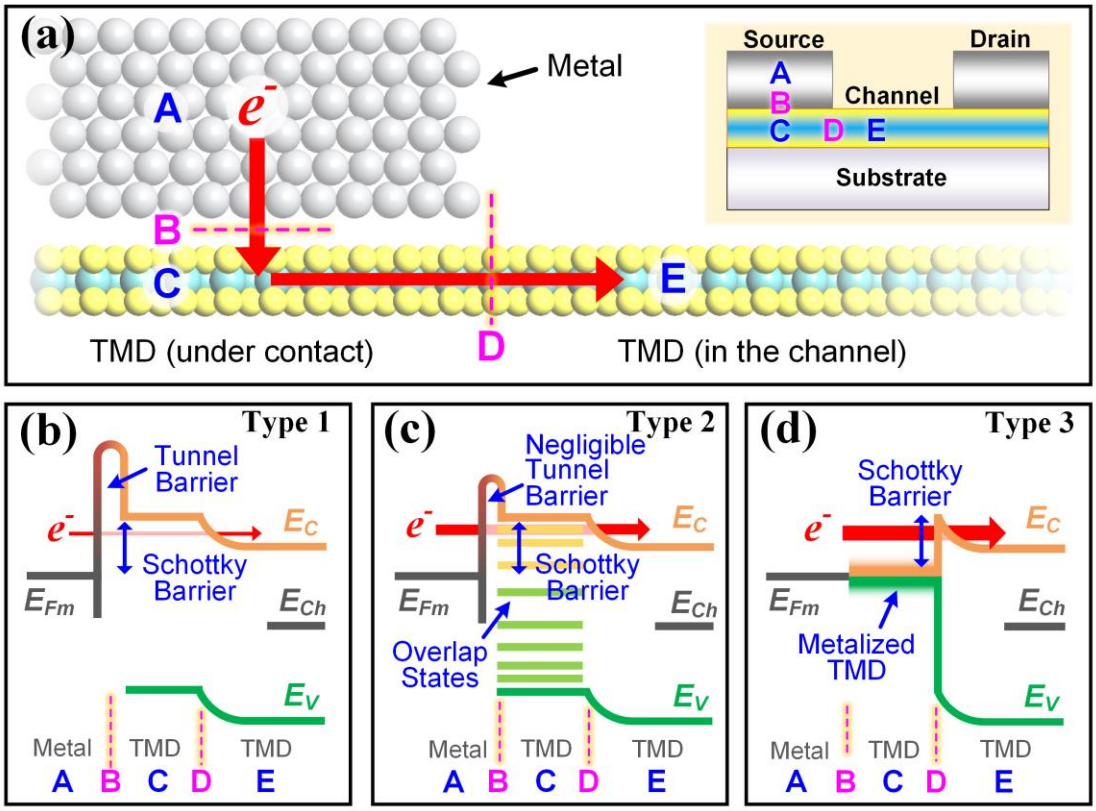


Figure 33: Schematics of different top-contact types.

(a) Schematic cross-sectional view of a typical metalMoS_2 contact (n-type top contact). A, C, and E denote the three regions while B and D are the two interfaces separating them. Red arrows show the pathway (A → B → C → D → E) of electron injection from contact metal (A) to the MoS_2 channel (E). The inset shows the source and drain contacts and the channel region in a typical backgated FET. (b)–(d) The three possible band diagrams of (a): metal contacts with (b) very weak bonding, (c) medium bonding, and (d) strong bonding. E_c, E_v, E_{Fm}, and E_{ch} represent conduction band edge, valence band edge, metal Fermi level, and channel potential, respectively

Hence, any top contact (**Figure 33a**) will form one of the three types of Schottky contacts (**Figure 33b-d**) (or their corresponding p-type contacts): *type 1*, metals with

negligible adhesion with 1L-TMDs; *type 2*, medium adhesion; and *type 3*, full adhesion. For *type 3*, as will be revealed later, these metals can form interface covalent bonds with 1L-TMDs (at interface B in **Figure 33a**), which strongly perturbs the band structure of 1L-TMD and results in vanishing of the 1L-TMD band gap (between B and D in **Figure 33d**) under metal. Therefore, the 1L-TMD is metalized and the Schottky barrier under the metal (at interface B in **Figure 33d**) vanishes, which leads to an Ohmic contact under the metal (at B) and a thinner Schottky barrier at the sourcedrain channel junction (interface D). Although the semiconducting properties of 1L-TMD under the contact metal are distorted, the channel region is not affected. Hence, this kind of contact is preferred for 1L-TMD devices.

2. Interface Modeling

As shown in **Figure 30b**, as well as **Figure 34**, metal-1L-TMD contact regions are modeled, which are periodic in the *x* and *y* directions and separated by vacuum in the *z* direction.

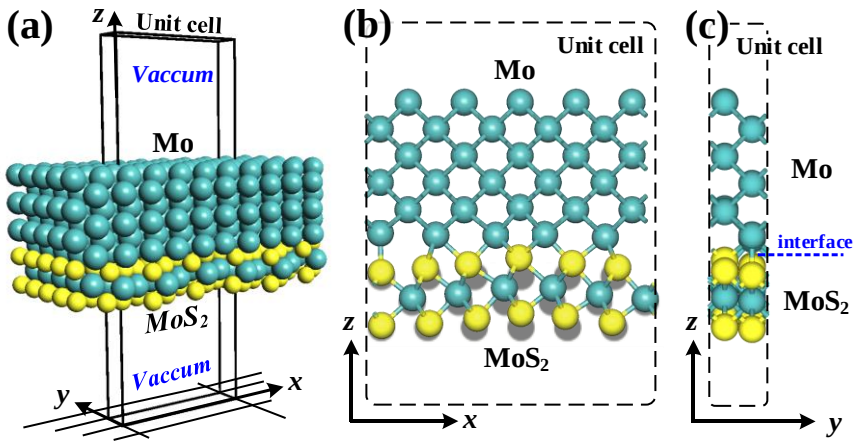


Figure 34: Optimized geometries of Mo top contacts to MoS_2.

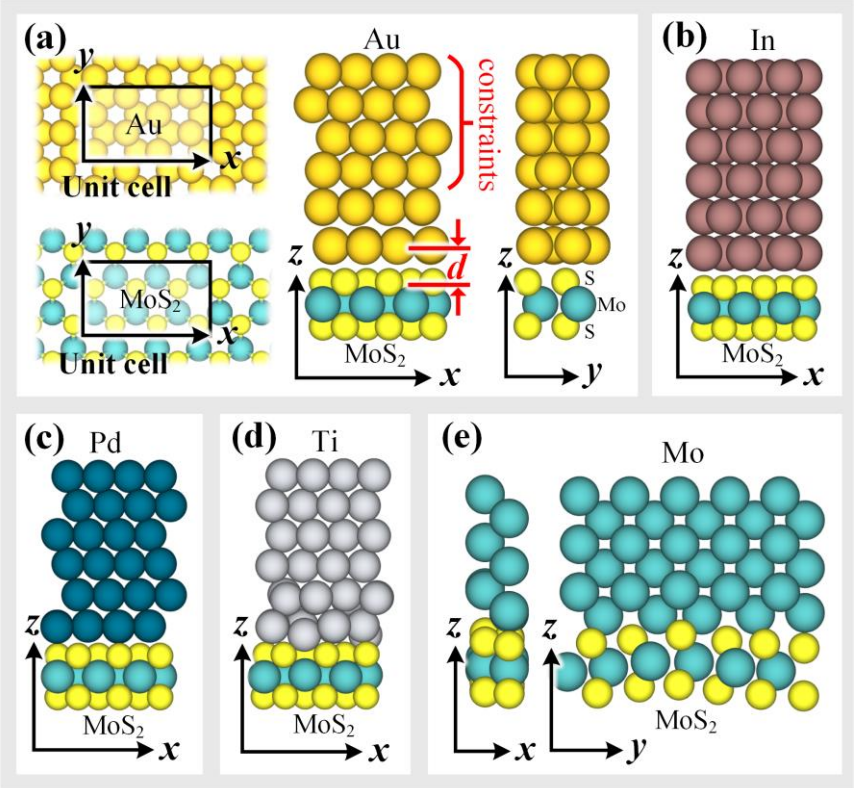


Figure 35: Optimized geometries of top contacts to MoS_2.

(a) Au-MoS_2 (in different views), (b) In-MoS_2, (c) Pd-MoS_2, (d) Ti-MoS_2, (e) Mo-MoS_2 (in different views). d is defined as the physical separation (the z component of the nearest core-tocore distance between the metal atoms and the chalcogenide atoms). Radii of the atomic spheres shown in (a)–(e) are fixed to the covalent radius of the elements, which is a measure of the size of an atom that forms part of one covalent bond. Hence, the touching of atomic spheres indicates the formation of covalent bonds (e.g., the Ti-S bond in (d)).

For all the top contacts, as shown in **Figure 35** and **Figure 36**, the contact region contains an intrinsic 1L-TMD monolayer and the close-packed surfaces of a metal [In(101), Ti(001), Au(111), Pd(111), Mo(001), or W(001)] extending to the sixth layer. These orientations are the most probable to be found in experiments. In this work, to emulate the

effect of upper layers in modeling, the third to sixth layers of metals from the interface are set as constraints (atoms with fixed locations), as shown in **Figure 35a**. 1L-TMD as well as first to second metal layers are allowed to relax. Although in real situations the contact metals consist of many layers, we restrict the simulation to only six layers of metal atoms because the obtained results do not change appreciably beyond this thickness.

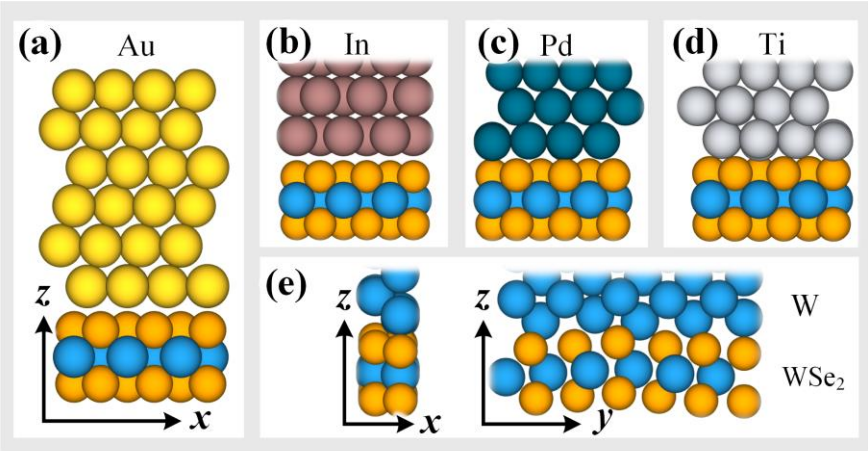


Figure 36: Optimized geometries of top contacts to WSe_2.

(a) Au-WSe_2, (b) In-WSe_2, (c) Pd-WSe_2, (d) Ti-WSe_2, (e) W-WSe_2.

3. DFT Calculations

The first-principles calculations are performed by DFT. Using DFT approaches, the properties of a many-electron system can be determined in the form of a spatially dependent electron density **[226]**, which makes it possible to incorporate quantum mechanical effects in the density function (3 degrees of freedom) rather than through many body wave functions (3 × N degrees of freedom).

The DFT approach employed in this work is the Kohn-Sham DFT **[227]**, where the problem of interacting electrons in a static external potential is reduced to a problem of non-

interacting electrons moving in an effective potential. The effective potential includes the external potential and the effects of the Coulomb interactions between the electrons, which is described by the exchange and correlation interactions.

Though, Kohn-Sham DFT has significant computational advantages over other ab initio methods, it is well known that the widely used exchange and correlation interactions of the generalized gradient approximation (GGA) **[228], [229]** or the local density approximation (LDA) **[230]** do not give accurate results for band gaps for some semiconductor materials. To ensure that the simulations are accurate, we first investigate the band structures of monolayers MoS_2 and WSe_2 calculated with either the LDA exchange correlation or the Perdew-Burke-Ernzerhof variant **[228], [229]** of GGA (PBE GGA), together with either the double-ζ polarized (DZP) basis set or the Hartwigsen-GoedeckerHutter (HGH) basis set for expanding the electronic density. The results show that LDA with DZP or HGH and GGA with HGH give a direct band gap of 1.8 eV for the monolayer MoS_2, which is consistent with results from experiments **[27]**, while for the monolayer WSe_2, only LDA gives a direct band gap of 1.6 eV that is consistent with the results obtained from both theory and experiments **[231]**.

The DFT-D2 results show consistent bandgaps with results from experiments **[27], [231]**. Since the valence band structures of bulk MoS_2 were recently measured by angle-resolved photoemission spectroscopy (ARPES) as reported in **[232]**, to further evaluate the simulation methodology, the calculated valence band structures of bulk MoS_2 by DFT-D2 with LDA (black curves) are superimposed on that of ARPES results (red dots) from **[232]**, as shown in **Figure 37**. It can be observed that the shapes of electronic dispersion spectrum of MoS_2 in simulations are in agreement with those from the experiments. This provides strong evidence that the methodology employed in this work can reproduce the electronic

spectrum correctly and the agreements between simulations and experiments are not just coincidental. Hence, LDA with HGH is chosen for all DFT simulations in this work.

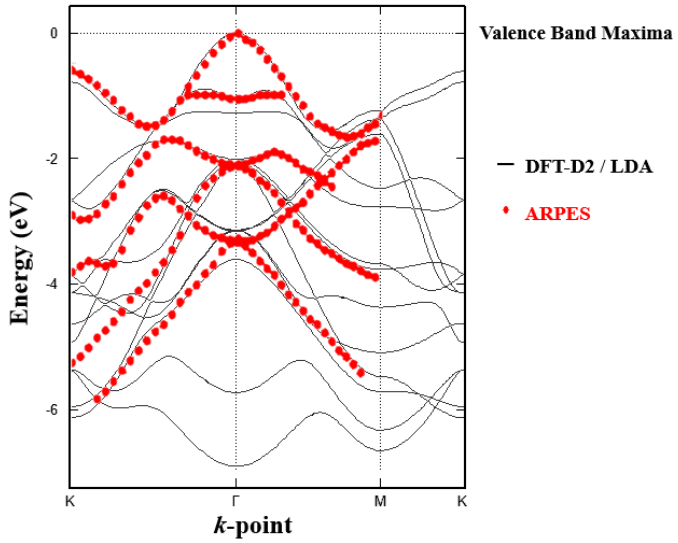


Figure 37: Comparison of calculated and measured band structures.

Valence band structures of MoS_2 by DFT-D2 with LDA is compared with experimentally reported ARPES result. The valence band maxima is set to zero energy.

Though accurate descriptions of covalent and ionic chemical bonds can be achieved with the settings as discussed above, they may fail to reproduce nonlocal dispersive forces, in particular, van der Waals forces, which are important in weakly bonded systems such as interfaces of two materials bonded with vdW, multilayer 2D materials, molecular crystals, and organic compounds **[233]**. As discussed in the introduction section, this problem has not been addressed in previous works on interfaces with 1L-TMDs **[1], [202]**, so the accuracy of the results from those works may be limited. Hence, the interfaces with 2D materials clearly require the development of new DFT methods designed to overcome this problem **[234], [235]**, by alterations to the functional or by the inclusion of additive terms, as shown for

graphene **[233]**. Pragmatic methods to address this problem have been provided by approaches such as DFT-D, DFT-D2 or DFT-D3 **[236]–[238]** and vdW-DF **[239]–[241]**. In DFT-D(2,3) approaches, a semi-empirical dispersion potential is added to the conventional Kohn-Sham DFT energy, where the potential is described via a simple pairwise force field and is optimized for popular DFT functionals.

Hence, in this work, DFT-D2 is adopted due to its higher accuracy, broader range of applicability, and lesser empiricism **[238]**. The calculations were performed using the Atomistix ToolKit (ATK) **[242]**. 8 × 16 × 1 k points were sampled in the Brillouin zone (BZ) of the top-contact region. The density mesh cutoff was 200 Ry and the maximum force was 0.05 eV/Å for geometry optimizations.

4. Contact Evaluation

Three major criteria (tunnel barrier, Schottky barrier, and orbital overlap) are analyzed to evaluate the electron injection efficiency of contacts as shown in **Figure 30d**, since they can sufficiently capture the essential interface characteristics of metal TMDs that determine their electrical behavior.

The first criterion—tunnel barrier—can be inferred from blocks I and II of **Figure 30** (the optimized geometry and the effective potential) calculated using DFT. A narrow and low tunnel barrier at the metal-1L-TMD interface can increase the electron injection efficiency.

Block I, optimized geometry, is the relaxed structure with minimum total energy, which reflects the nature of ideal interfaces theoretically. Physical separations (d) (defined in **Figure 35**) are measured from optimized geometries. d is directly related to the width ($\leq d$) of the tunnel barrier between metal and 1L-TMD.

In block II, the effective potential (V_{eff}) of an electron represents its interaction with

other electrons and the external electrostatic field. V_{eff} is calculated by $V_{eff}(n) = V_H(n) + V_{xc}(n) + V_{ext}$, where $V_H(n)$ is the Hartree potential due to the mean-field electrostatic interaction, $V_{xc}(n)$ is the exchange-correlation potential caused by the quantum mechanical nature of the electrons, and V_{ext} represents other electrostatic interactions in the system. The tunnel barrier height can be characterized by the peak of V_{eff} at the interface, which is noted as effective tunnel barrier height ($\Phi_{TB;eff}$) (defined in **Figure 38a**).

The Schottky barrier can be determined by blocks III and IV (the band structure and the partial density of states)

In block III, the band structure (or energy dispersion) can be calculated for the metal-1L-TMD contact system. By comparing the original band structure of MoS_2 without contact and the new band structure after contact, the shift of Fermi level (E_F) can be identified, as can the Schottky barrier.

In block IV, the partial density of states (partial DOS or PDOS) is the density of states on specified atoms and orbitals. The Schottky barrier can also be measured by the energy difference between conduction or valence band edge (E_c or E_v) of 1L-TMD and E_F of the metal-1L-TMD contact system. As shown in **Figure 30c,d**, (electron) orbital overlap (in other words, bond formation) is evaluated by blocks IV, V, and VI in **Figure 30c**. By comparing the PDOS on 1L-TMDs before and after contact formation, overlap states can be found, the density of which indicates the strength of orbital overlaps in the energy domain. In block V, valence electron density (at the interfaces) indicates the strength of overlapped electron orbitals in the real space. High (valence) electron density at the interfaces allows sufficient injection of charge into the 1L-TMD layer **[202]**. In block VI, bond Mulliken population is the overlap population of electrons for pairs of atomic orbitals **[243]**. This result gives a visual and quantitative evaluation of the orbital overlap. Bond Mulliken

populations n have a typical range of $0 \leq n \leq 1$, where $n = 0$, $0 < n < 1$, and $n = 1$ indicate ionic bond, partial covalent bond, and full covalent bond, respectively. The population indicates the strength of the covalent bond, or in other words, the strength of the orbital overlaps in terms of shared electron numbers. For example, the Mo-S (W-Se) covalent bond in MoS_2 (WSe_2) has a population of 0.53 (0.50).

5. Tunnel Barriers

The tunnel barrier between a metal and TMD is characterized by its width and height, which are evaluated by the physical separation (d, measured from the optimized geometry) and effective tunnel barrier height ($\Phi_{TB;eff}$), respectively.

To evaluate the tunnel barrier widths, optimized geometries of top contacts are simulated and shown in **Figure 35** and **Figure 36**. The physical separations (d) between the metal and 1L-TMD atoms are defined as shown in **Figure 35** and **Figure 36**. For all of the top contacts, d is calculated and plotted in **Figure 38b**. Because of the smaller atomic sizes of MoS_2 compared to that of WSe_2, top contacts to MoS_2 have smaller physical separations. For low-WF metal (In, Ti) top contacts to 1L-TMD, Ti gives much smaller d (1.51 Å to MoS_2 and 2.13 Å to WSe_2) than that of In (2.58 Å to MoS_2 and 2.67 Å to WSe_2). While for high-WF metal (Au, Pd) top contacts, Pd-1L-TMD top contacts give smaller physical separations than Au-1L-TMD top contacts, as shown in **Figure 38b**.

Mo and W top contacts to 1L-TMD are evaluated in the same manner. However, d values of Mo-MoS_2 and W-WSe_2 top contacts are extremely small (1.25–1.42 Å) compared to all of the other metal-1L-TMD top contacts (1.51–2.87 Å). Those small physical separations may lead to extremely thin tunnel barriers and strong orbital overlaps. Moreover, it can be clearly seen from **Figure 35e** that atoms in 1L-TMDs are dragged by Mo (W) atoms to form Mo-S (W-Se) interface bonds, resulting in the breaking of 1L-TMD

periodicity by deformation. Hence, strong disturbing of 1L-TMD band structures (which will be shown later in **Figure 41c**) can be expected.

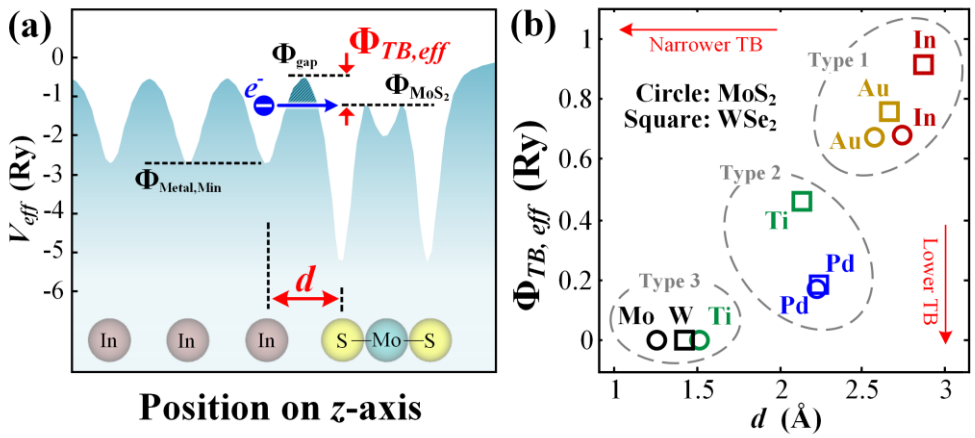


Figure 38: Evaluation of the tunnel barriers at the contacts.

(a) Plot of minimum effective potential (V_{eff}) versus z position for In-MoS_2 top-contact. Φ_{MoS_2} is the V_{eff} of the Mo-S bond orbitals and thereby the effective tunnel barrier height ($\Phi_{TB;eff}$) is defined as the minimum barrier height that an electron from the metal has to overcome if it has the same potential energy as Φ_{MoS_2}. Hence, $\Phi_{TB;eff}$ can be calculated as the V_{eff} difference between the vdW gap (Φ_{gap}) and MoS_2 (Φ_{MoS_2}). $\Phi_{metal;min}$ denotes the minimum V_{eff} that an electron can have in the metal. It is worth noting that in some metals (such as Au) $\Phi_{metal;min}$ can be higher than Φ_{MoS_2} (thus, electron energy is always higher than that of Mo-S bond orbitals), in which case $\Phi_{TB;eff}$ is calculated as $\Phi_{TB;eff} = \Phi_{gap} - \Phi_{metal;min}$. $\Phi_{TB;eff}$ vanishes to zero when $\Phi_{metal;min}$ or Φ_{MoS_2} is higher than Φ_{gap}. *d* is defined as the physical separation (the z component of the nearest core-to-core distance between the metal atoms and the chalcogenide atoms). (b) $\Phi_{TB;eff}$ versus d plot for various top contacts.

To evaluate the tunnel barrier heights, effective potentials (V_{eff}) are calculated. The minimum effective potential (V_{eff}) along the z direction for the In-MoS_2 top contact is shown in **Figure 38a** as an example. As illustrated by **Figure 38a**, the effective tunnel barrier height ($\Phi_{TB;eff}$) can be measured from V_{eff} and $\Phi_{TB;eff}$ of each contact, as plotted in **Figure 38b**. Similarly, top contacts to MoS_2 have lower tunnel barriers than those of top contacts to WSe_2. According to the results, Au- and In-1L-TMD contacts have high $\Phi_{TB;eff}$ (0.67–0.92 Ry), while for Mo- and Ti-MoS_2 and W-WSe_2 top contacts there is nearly no barrier ($\Phi_{TB;eff}$ = 0 Ry) at the interface, indicating high electron injection efficiency and thus low contact resistance.

Based on the evaluation of the tunnel barriers, the types of contacts (**Figure 33b-d**) can be preliminarily predicted, as shown by type 1, type 2, and type 3 in **Figure 38b**.

6. Schottky Barriers and Fermi Level Pinning

To further evaluate the top contacts and find the SBs, PDOS are calculated and shown in **Figure 39** and **Figure 40**, and compared to 1L-TMD without contacts.

In **Figure 39b,c,e,f** (**Figure 40b,c,e,f**), the position of E_F is shifted towards the original conduction band (E_c) indicating that MoS_2 (WSe_2) is doped n type by Au, In, Ti, or Mo (W). The E_F of the Pd-MoS_2 top contacts lie at the middle of the MoS_2 band gap (**Figure 39d**), indicating that MoS_2 is still nearly intrinsic with the Au top contact. In contrast, E_F is close to the original E_v of monolayer WSe_2. Hence, the Pd-WSe_2 top contact is shown to be a p-type contact (**Figure 40d**). This is the only p-type top contact found in this study, in agreement with experimental results on Pd-contacted MoS_2 devices **[25]**.

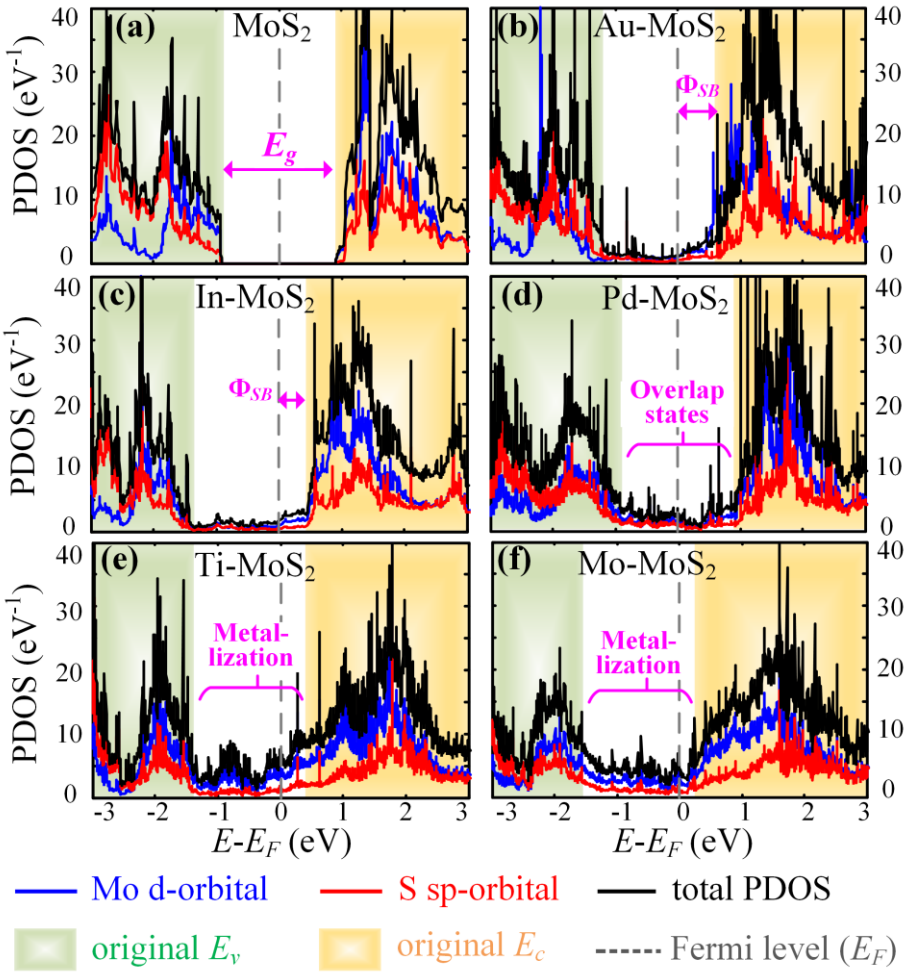


Figure 39: Partial density of states (PDOS) of top contacts to MoS_2.

PDOS is DOS on specified atoms and orbitals, for example, Mo-d (d orbital on Mo). (a) only MoS_2, (b) Au-MoS_2, (c) In-MoS_2, (d) Pd-MoS_2, (e) Ti-MoS_2, (f) Mo-MoS_2. E_F denotes Fermi level.

By measuring the energy difference between E_F and the original E_c, the Schottky barrier height (Φ_{SB}) for each contact can be estimated, as indicated in **Figure 39b,c** and **Figure 40b,c**. However, more precise results can be achieved by the analysis of band structures. In **Figure 41**, the band structures of Au-, Ti-, and Mo-MoS_2 systems are plotted (in gray). The original band structure of MoS_2 without contact is also plotted for reference (red curves),

which is superimposed on the new band structure (gray curves) such that old and new subbands align.

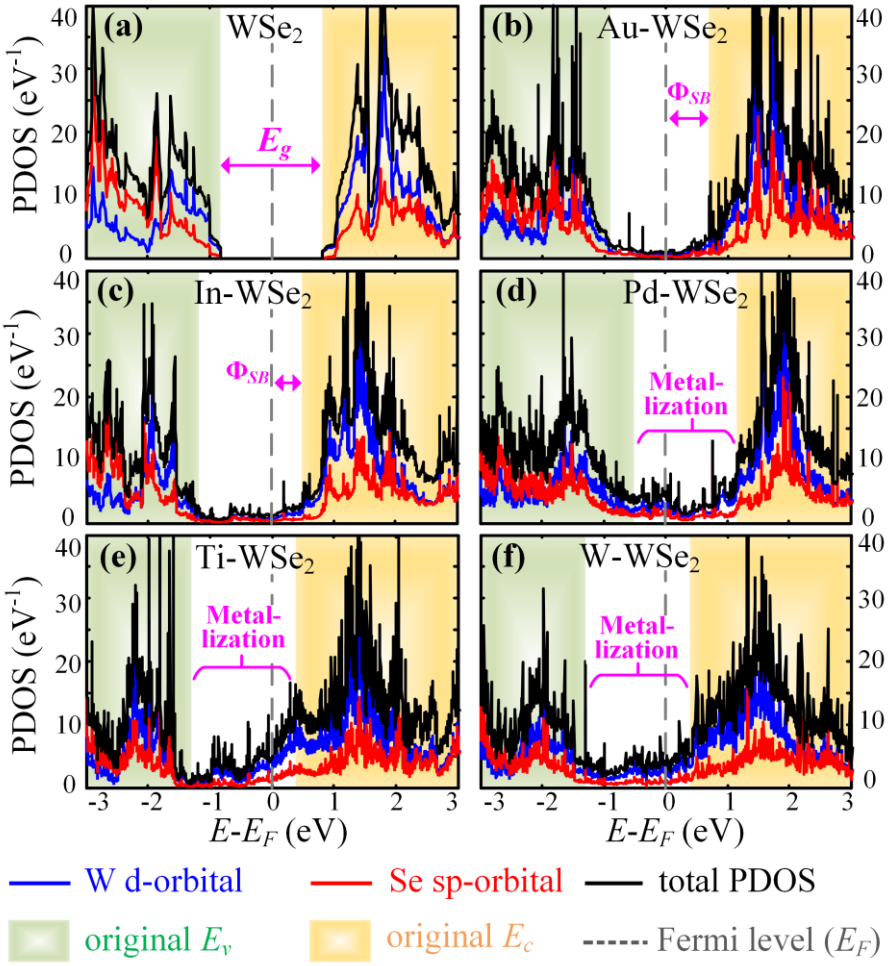


Figure 40: PDOS of top contacts to WSe_2.

(a) only WSe_2, (b) Au-WSe_2, (c) In-WSe_2, (d) Pd-WSe_2, (e) Ti-WSe_2, (f) W-WSe_2. E_F denotes Fermi level.

Φ_{SB} in each plot is then measured accordingly. For example, in Au- and Ti-MoS_2 top contacts, the Schottky Barriers are 0.62 and 0.33 eV, respectively, from DFT simulation. Using this approach, Φ_{SB} for all of the top contacts is calculated and listed in **Figure 42**.

According to our recent experimental work (under review), the extracted Schottky barrier between Ti and monolayer MoS_2 varies between 0.3 and 0.35 eV measured from 6 monolayer devices, which is in agreement with the simulation results (0.33 eV).

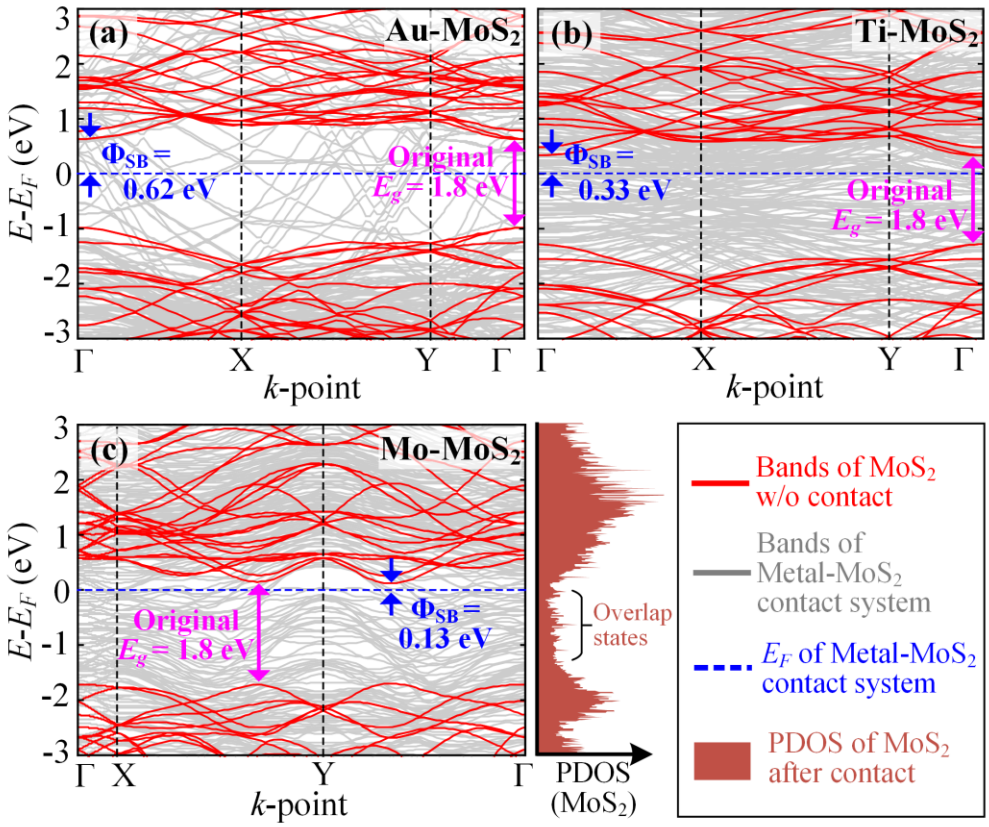


Figure 41: Band structures of some top contacts.

(a) Au-MoS_2 system, (b) Ti-MoS_2 system, and (c) Mo-MoS_2 system. The original band structure of MoS_2 without contact is also plotted for reference (red curves), which is superimposed on the new band structure (gray curves) such that old and new subbands align. The Schottky barrier (Φ_{SB}) is marked in blue. Note that the symmetric points (Γ, X, and Y) are different between (a), (b), and (c) due to different dimensions of the unit cells. PDOS of MoS_2 after contact by Mo is also shown in (c).

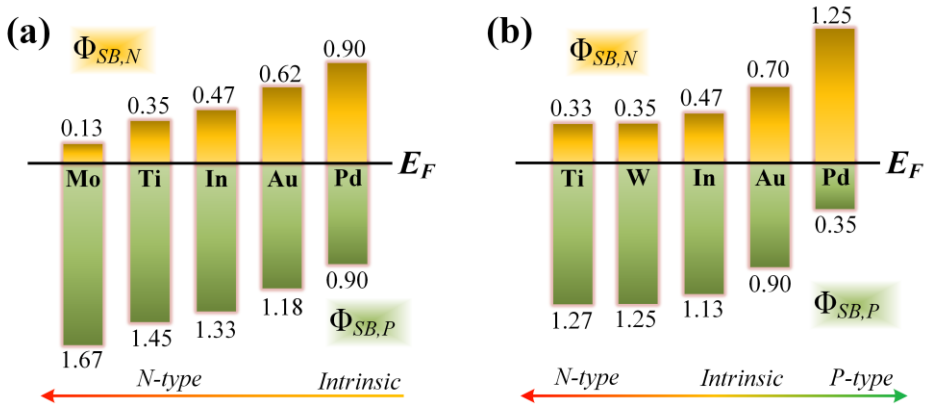


Figure 42: Φ_{SB} of all of the top contacts.

(a) MoS_2 top contacts and (b) WSe_2 top contacts. $\Phi_{SB;N}$ ($\Phi_{SB;P}$) denotes n type (p type) SB for electrons (holes)

Moreover, despite the high WF (4.5 eV) of Mo (**Figure 32**), the Fermi level is pinned at only 0.13 eV below the original E_c of intrinsic monolayer MoS_2 (**Figure 42**), indicating a Schottky barrier of 0.13 eV at interface D in **Figure 33d**. This Schottky barrier height is much lower than that of the Ti-MoS_2 top contact (0.33 eV, as shown in **Figure 41b**), although Ti has a smaller WF that is also closer to the electron affinity of MoS_2 (4.3 eV, **Figure 32**). This also indicates that the properties of contacts to 2D materials cannot be intuitively predicted by WF values.

Though selected metals form strong hybridization at the interfaces and therefore suppress the tunnel barrier, Fermi level pinning happens due to the changing of the work function of the metal layer at the interfaces (into the metal-MoS_2 alloy's work function) **[2]** as well as the creation of gap states from the weakened intralayer S-Mo bonding **[223]**. Such effects can significantly impact the Schottky barrier height (SBH).

Since the MoS_2 is monolayer, its properties can be easily distorted by the strong orbital overlaps (covalent bonds), which create overlap states. Thus, the electronic properties of the

MoS_2 under the contact change. In other words, the compound (Mo-MoS_2 alloy) at the interface can be expected to be a new material, which has a much lower WF compared to that of the unalloyed MoS_2 in the channel region (**Figure 33a**). Hence, the unalloyed MoS_2 (near the contacts) is n-type doped as if it is contacted to a low-WF metal. This phenomenon has also been confirmed in the simulation of the Mo contact on multilayer MoS_2 **[6]** (and also in **Section E.1**).

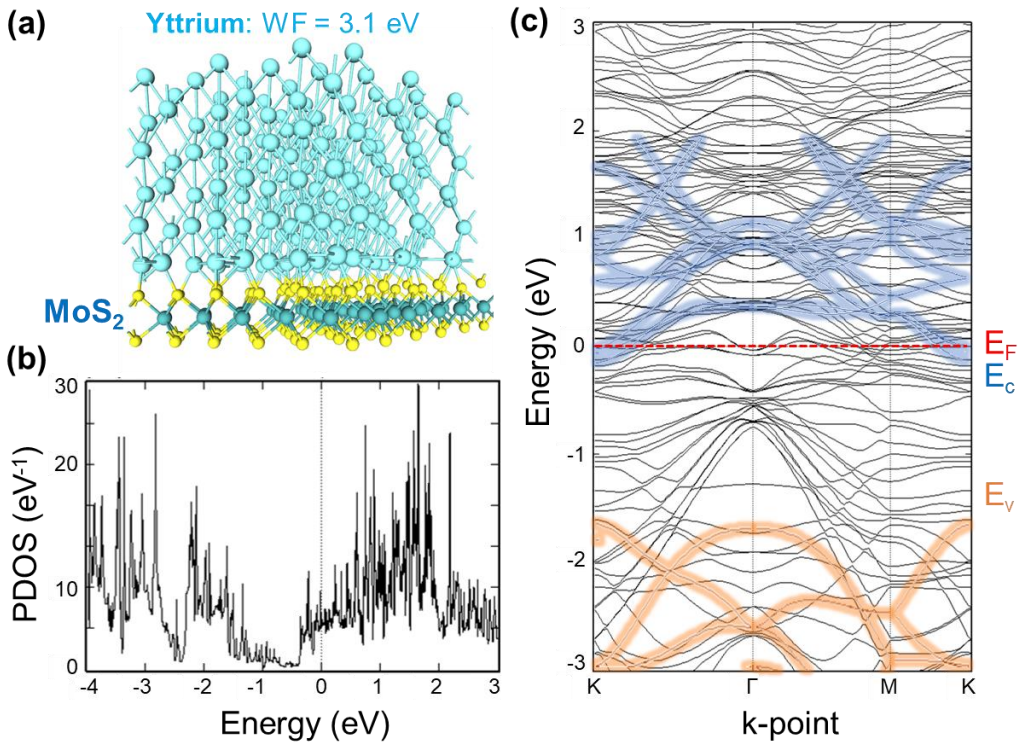


Figure 43: Interface properties of Y-MoS_2 contact.

(a) Relaxed geometry, showing formation of covalent bonds (hybridization); (b) partial DOS on MoS2; (c) band structure of MoS_2 (colors) and Y-MoS_2 (black).

DFT simulations tell that some extremely low-WF metals can form zero SB on MoS_2. For example, Yttrium, with low WF of 3.1 eV, when form Yttrium-MoS_2 interface, shows

strong hybridization, zero Schottky barrier and zero tunnel barrier (**Figure 43**).

It is also important to note that the study of the Fermi level pinning at the metal-TMD interface requires careful treatment of the vdW interaction between them, which is usually missing in studies of 2D interfaces. Using pure LDA, no reliable predictions can be made due to its limitations in handling vdW interactions **[234]**. In particular, LDA does not correctly reproduce the interlayer binding energies **[235]**. DFT-D functionals give the closest interlayer binding energy results for layered MoS_2 and WSe_2 with respect to the comprehensively and experimentally tested random-phase approximation method, compared with LDA, PBE GGA, and vdW-DF **[234]**. Also, considering its lower computational demands, DFT-D is more useful for describing vdW interaction. Hence, the adoption of the DFT-D2 (newer version of DFT-D) functional in this work is highly necessary and suitable, and thus the results are more reliable

7. Orbital Overlapping (Hybridization)

Because of the lack of orbital overlaps, Au- and In-1L-TMD top contacts are typical Schottky contacts (*type 1* in **Figure 33b**). In contrast, for Pd-MoS_2 top contacts (**Figure 39d**), overlap states can be found in the original band gap of MoS_2. This indicates that the Pd-MoS_2 top contact is *type 2* (**Figure 33c**). As illustrated in **Figure 33c**, these overlap states contribute to the electron or hole injection from the metal. As shown earlier, the overlap of Ti and S atomic spheres can be clearly observed from the optimized geometry of the Ti-MoS_2 top contact **Figure 35d**, which indicates the high possibility of covalent bond formation between Ti and MoS_2. This is proved by **Figure 39e**, where the high PDOS spreads all over the original band gap, which represents the overlap states corresponding to the covalent bonds. Hence, Ti-MoS_2 has an Ohmic interface (at B in **Figure 33d**), where the band gap vanishes and the MoS_2 region under the contact metal (**Figure 33a**) is metallized.

Similar results are also found in Mo-MoS_2, Ti-WSe_2, Pd-WSe_2, and W-WSe_2 top contacts. Hence, although Mo and W do not have suitable WFs for MoS_2 and WSe_2, respectively, both Mo-MoS_2 and W-WSe_2 top contacts have Ohmic interfaces (B in **Figure 33d**). These results can be found only by atomic level modeling (i.e., DFT) and cannot be inferred intuitively from analytical Schottky barrier theory.

As shown in **Figure 41b,c**, most of the original MoS_2 bands (red) are disturbed by Ti or Mo contact, forming new bands (gray) that extend into the original band gap, which correspond to the covalent bands with overlap states, while most of the MoS_2 bands in the Au-MoS_2 system remain the same as in pure MoS_2 (**Figure 41a**), indicating the lack of orbital overlaps. It is important to note that electrons on the overlap states in the Ti- and Mo-MoS_2 systems are not localized, so that the metal will not degrade the conductivity of MoS_2 under the contact. This can be confirmed by the shapes of the energy bands of the Ti- and Mo-MoS_2 system (gray curves) in **Figure 41b,c**, where most of the energy bands have high enough curvature (indicating small effective mass) for efficient carrier transport. Valence electron densities of top contacts are calculated and shown in **Figure 44**. The minimum values of the x-y plane averages (ρ_m) at the interfaces are measured and marked on the curves or contours. The Au and In contacts give relatively lower ρ_m, indicating weak adhesion and, thus, weak orbital overlaps. For Pd top contacts, the corresponding values are better (greater than 0.02 $bohr^{-3}$), due to stronger overlap. Ti-1L-TMD contacts have high ρ_m values of 0.033 and 0.029 $bohr^{-3}$, implying that Ti has the possibility to achieve strong orbital overlaps with monolayer MoS_2 and WSe_2, leading to low contact resistance. Moreover, Mo-MoS_2 and W-WSe_2 have even higher ρ_m at the interfaces than the others, so that the Mo and W top contacts can be expected to have the highest electron injection efficiency among all of the top contact metals.

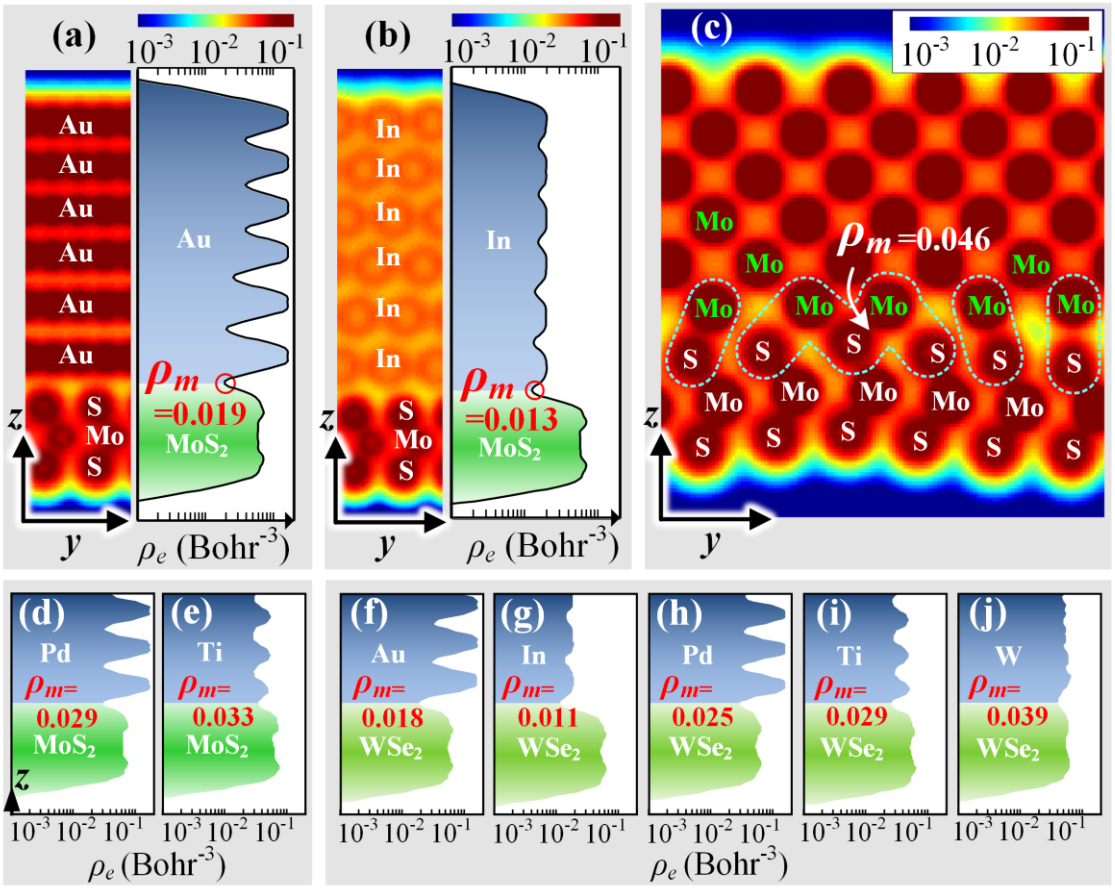


Figure 44: Valence electron densities (bohr^{-3}) of top contacts.

(a) Au-MoS_2, (b) In-MoS_2, (c) Mo-MoS_2, (d) Pd-MoS_2, (e) Ti-MoS_2, (f) Au-WSe_2, (g) In-WSe_2, (h) Pd-WSe_2, (i) Ti-WSe_2, (j) W-WSe_2. Panel (c) and the left-hand contours in (a) and (b) show average density alongx projected onthey-z plane. Panels (d)–(j) and the right-hand plots in (a) and (b) show average electron density value in the x-y planes normal to the z axis (ρ_e). ρ_m in each panel indicates the minimum x-y plane average electron density at each interface (in units of bohr^{-3}).

These predictions can also be confirmed by Mulliken population analysis. The maximum bond Mulliken populations calculated from all of the top-contact interfaces are listed and

sorted in **Figure 45a**, compared with values inside intrinsic MoS_2 and WSe_2. These two sequences of populations indicate the sequences of covalent bond strength. According to **Figure 45a**, the populations of Ti-S, Mo-S, and W-Se bonds at the interfaces (0.59, 0.67, 0.51) can be even higher than that of Mo-S (W-Se) bonds inside MoS_2 (WSe_2) [0.53 (0.50)], which implies that stronger covalent bonds are formed at the interfaces than in 1L-TMDs. Particularly, to prove the strong orbital overlaps of Ti-MoS_2 top contacts, the bond Mulliken populations of all Ti-S bonds at the Ti-MoS_2 top contact interface are shown in **Figure 45b**, which range from 0.42 to 0.59 and are much higher than that for In, Au, and Pd.

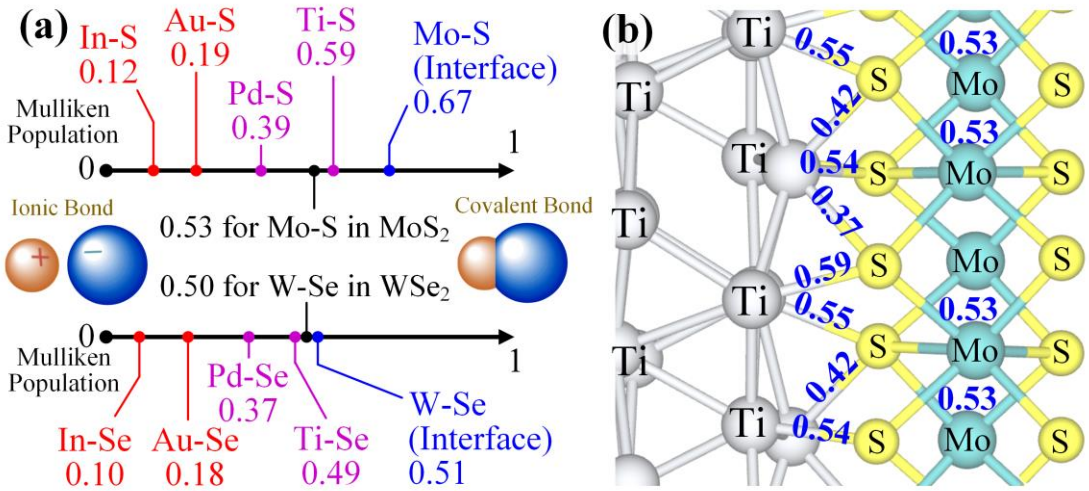


Figure 45: Bond Mulliken populations of top contacts.

(a) Maximum bond Mulliken populations (on a scale of 0 to 1) of top-contact interface bonds (colored numbers) compared to that of Mo-S (W-Se) bonds inside mTMDs (black numbers). (b) Bond Mulliken populations of the Ti-MoS_2 top contact. Population values are marked beside each interface bond. Population values of Mo-S bonds are also marked in MoS_2

It is worth noting that the DFT results of the strong hybridization cases (**Figure 25f**) are

based on the assumption of perfect interfaces. In practice, the close-to-perfect interfaces require the removal or prevention of surface impurities (such as resist residues), as well as an annealing process. For example in graphene, during annealing, the carbon atoms can dissolve into the contact metal (Ni or Co) forming strong covalent bonds, which contributes to much smaller contact resistance **[244]**.

8. Summary of Top Contacts

Based on the above analysis on tunnel barrier, Schottky barrier, and orbital overlap, all of the top contacts can be categorized as follows, as summarized in **Figure 46**.

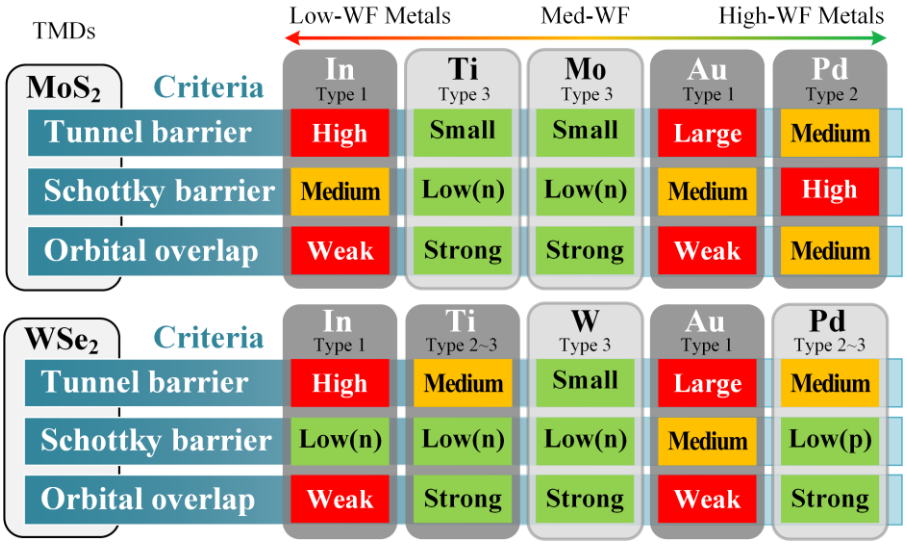


Figure 46: Summary of metal-1L-TMD top-contact.

Electron injection efficiency is evaluated, in terms of orbital overlap, Schottky barrier, and tunnel barrier.

i. Au and In contacts are *type 1*. Between these two metals, Au is favored for its better orbital overlap on MoS_2 **[23]** than that of In, while In is better in terms of Schottky barrier height and more applicable to WSe_2 **[7]**.

ii. Although Pd is a *type 2* metal on MoS_2, the Schottky barriers from Pd to MoS_2 are relatively higher (0.90 eV for both n- and p-type SB). Hence, Pd is not suitable for MoS_2. However, compared to the Pd-MoS_2 contact, Pd-WSe_2 provides a much lower p-type Schottky barrier (0.35 eV) and much higher overlap states or metallization, which makes Pd-WSe_2 to be beyond *type 2* and is somewhere between *type 2* and *type 3*.

iii. Ti-MoS_2 top contact can be expected to have excellent electron injection efficiency. It can be categorized as *type 3* due to the strong metallization and absence of TB at the interface. Ti also provides strong metallization to WSe_2, but an unexpected tunnel barrier degrades its performance on contacting WSe_2. Hence, the Ti-WSe_2 top contact is rated between *type 2* and *type 3*.

iv. Based on DFT simulations presented above, Mo shows great potential as a high-quality contact metal for MoS_2 and is classified as *type 3*. Mo is superior in terms of Schottky barrier (0.13 eV) than that of Ti-MoS_2 top contact (0.33 eV). However, the PDOS near the Fermi level of MoS_2 under the Mo contact (marked by the purple brace in **Figure 39f**) is slightly lower than that of MoS_2 under the Ti contact (**Figure 39e**), which may counter Mo's advantage of lower Schottky barrier compared to that in the case of Ti. This is in agreement with my recent measurements on Mo-MoS_2 contacts **[6]** (and also in **Section E.1**), where Mo and Ti contacts exhibit very similar contact resistances.

v. Similar to Mo-MoS_2, W-WSe_2 is also an excellent *type 3* contact. Despite its high WF, W provides n-type contact on WSe_2 due to Fermi level pinning since it forms an alloy whose WF is close to the electron affinity of WSe_2.

D. Edge Contacts and Multilayer TMDs

One option to overcome the vdW gap is to take advantage of edge-contacts. In fact, edge-contacts to monolayer graphene have been modeled **[245]** and shown **[205]** to perform

better than top-contacts. In this section, DFT results will show that edge-contacts lead to shorter bonding distance with stronger hybridization (orbital overlap) than top-contacts, and transport simulations show that incorporation of additional interfacial species (such as oxygen) can further help in improving bonding and increasing the transmission **[205]**. The reported contact resistance for Cr edge-contact to monolayer graphene is about 150 Ω·μm, in good agreement with the value of 118 Ω·μm predicted from simulations **[205]**. For TMD semiconductors, edge contacts can also be advantageous compared to top contacts. This has been verified by DFT simulations in this section for both monolayer **[1], [2]** and multilayer TMDs **[5]**. The main reasons are the stronger orbital overlaps and the reduction of tunnel barriers.

1. Edge Contacts to 1L-TMDs

In this section, Au, In, Pd, and Ti are chosen for modeling edge-contact configurations. There are many ways to terminate the 1L-TMD layers at the edges depending on the contact orientations. In particular, armchair termination of MoS_2 leads to semiconducting behavior, and its electronic properties are weakly dependent on the ribbon width, while the entire zigzag MoS_2 ribbon exhibits metallic behavior **[246]**. Hence, to preserve the semiconducting properties of 1L-TMDs as much as possible, which is also the worst case for electron injection due to the band gap, we choose the armchair edges to form interfaces (shown in **Figure 47**). Four out of six 1L-TMD unit cells on the left are set as constraints (**Figure 47a**) to emulate the effect of a long 1L-TMD layer on the left (same as the configuration for metal-graphene edge contacts **[245]**), while all other atoms (including four layers of metal atoms) are allowed to relax.

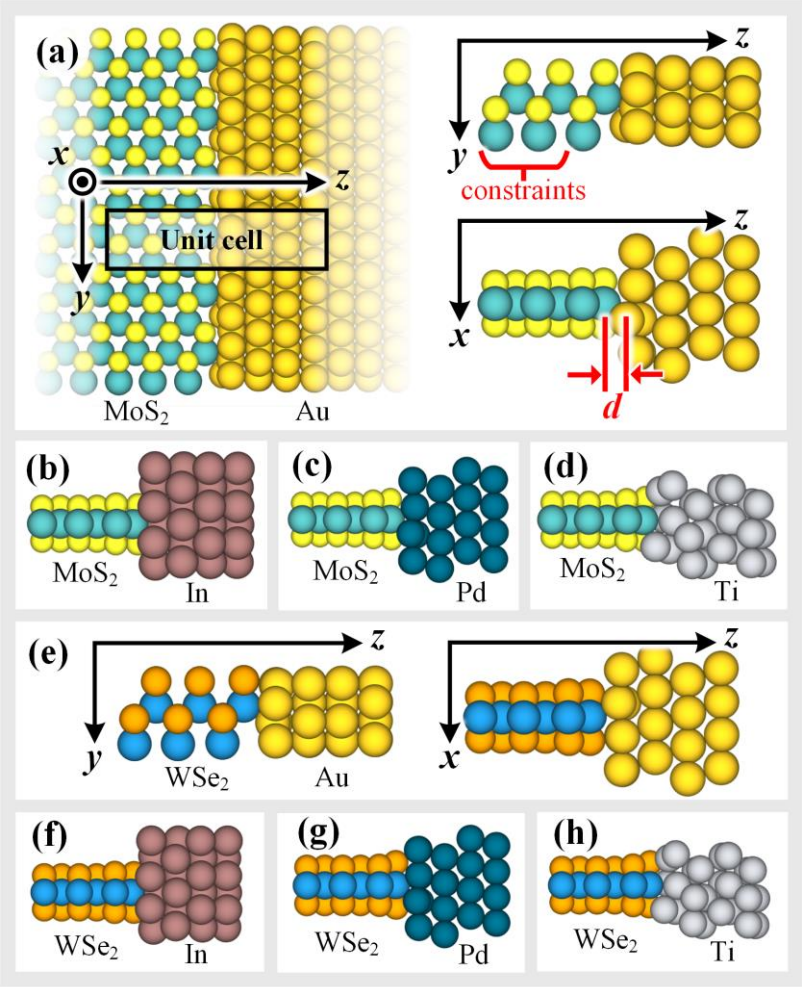


Figure 47: Optimized geometries of edge contacts.

(a) Au-MoS_2 (in different views), (b) In-MoS_2, (c) Pd-MoS_2, (d) Ti-MoS_2, (e) Au-WSe_2 (in different views), (f) In-WSe_2, (g) Pd-WSe_2, and (h) Ti-WSe_2. The large-volume overlaps of metal and chalcogenide atomic spheres exist in every edge contact [in (a)–(h)], indicating the formation of strong covalent bonds. Hence, physical separations in edge contacts (Table 5) are much smaller than that of top contacts in Figure 35 and Figure 36 due to the covalent bonds formed between mTMD and metals.

The calculations were performed using the Atomistix ToolKit (ATK) **[242]**. 8 × 8 × 1 k points were sampled in the Brillouin zone (BZ) of the top-contact region. The density mesh

cutoff was 200 Ry and the maximum force was 0.05 eV/Å for geometry optimizations.

In all of the simulated metal-1L-TMD edge contacts, the physical separations (*d*) are much smaller (**Table 5**) than that of top contacts (**Figure 38b**), because of the formation of covalent bonds between the metal and 1L-TMD as shown in **Figure 47**, where overlaps of metal and chalcogenide atomic spheres can be found in each of the edge contacts. Hence, tunnel barrier widths are reduced using edge-contact configuration and edge contacts have a high possibility of covalent bond formation between metals and 1L-TMDs.

Table 5: Evaluation of tunnel barriers at edge-contact interfaces.

	MoS_2				WSe_2			
	In	Ti	Au	Pd	In	Ti	Au	Pd
d (Å)	1.38	0.84	1.70	1.72	1.54	1.32	2.18	1.89
$\Phi_{TB,eff}$ (Ry)	0.00	0.00	0.54	0.12	0.00	0.00	0.12	0.00

As shown in **Figure 48**, V_{eff}'s along the z axis are smoother at the interfaces with smaller tunnel barriers (**Table 5**) compared to those for top contacts. For example, the Au-MoS_2 top contact has an effective tunnel barrier height of 0.67 Ry (**Figure 38a**), while the height in the Au-MoS_2 edge contact is reduced to 0.54 Ry (**Figure 48a**), which allows higher electron injection efficiency than that of top contacts. Moreover, in the In-MoS_2 edge contact, the $\Phi_{TB,eff}$ vanishes (**Figure 48b**), compared to that of the top contact. This phenomenon is also found in Pd edge contacts.

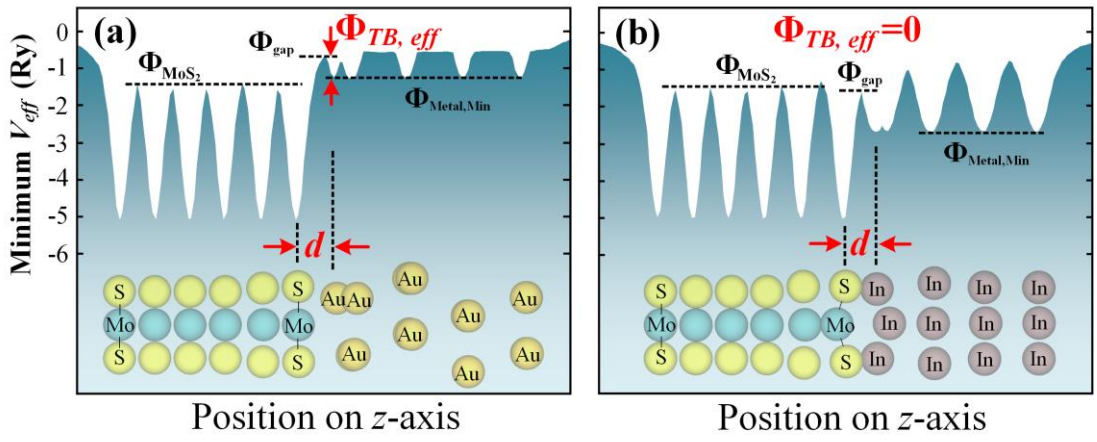


Figure 48: Minimum V_{eff} at edge contacts.

(a) Au-MoS_2 edge contact and (b) In-MoS_2 edge contact. Φ_{MoS_2} is the V_{eff} of the Mo-S bond orbitals and thereby the effective tunnel barrier height ($\Phi_{TB;eff}$) is defined as the minimum barrier height that an electron from the metal has to overcome, if it has the same potential energy as Φ_{MoS_2}. Hence, $\Phi_{TB,eff}$ can be calculated as the V_{eff} difference between the vdW gap (Φ_{gap}) and MoS_2 (Φ_{MoS_2}). $\Phi_{metal;min}$ denotes the minimum V_{eff} that an electron can have in the metal. It is worth noting that in some metals (such as in (a)) $\Phi_{metal,min}$ can be higher than Φ_{MoS_2} (thus, electron energy is always higher than that of Mo-S bond orbitals), in which case $\Phi_{TB;eff}$ is calculated as $\Phi_{TB,eff} = \Phi_{gap} - \Phi_{metal,min}$. d is defined as the physical separation (the z component of the nearest core-to-core distance between the metal atoms and the chalcogenide atoms). Though *d* does not vanish, $\Phi_{TB;eff}$ can vanish, when $\Phi_{metal,min}$ or Φ_{MoS_2} is higher than Φ_{gap}, such as in (b).

PDOS of edge contacts are shown in **Figure 49**. SBs and band gaps are absent in all of the edge contacts. The metallization is mainly due to stronger orbital overlaps, which induce high density of states in the original band gaps.

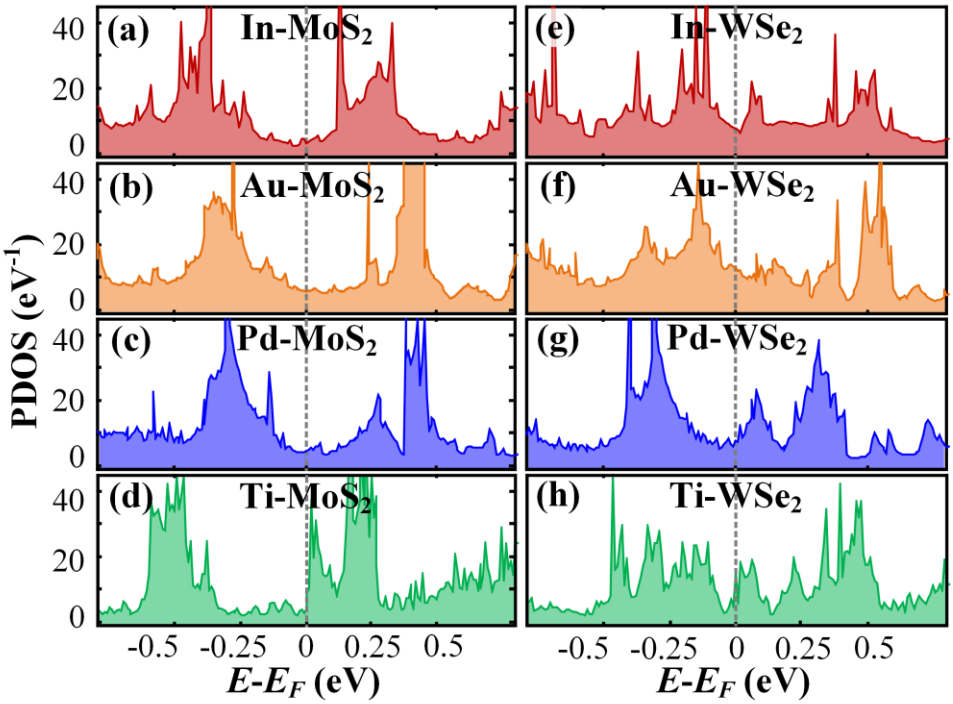


Figure 49: PDOS of 1L-TMD near E_F of edge contacts.

(a)–(d) MoS_2 and (e)–(h) WSe_2. Because of orbital overlaps (covalent bonds) at the interfaces, all the TMDs in edge contacts have overlap states in the original band gaps and near E_F, so that TMDs are metallized by edge contacts.

Minimum valence electron densities at the interfaces (ρ_{min}) are increased compared to that of most of the top contacts, as shown in **Figure 50a,b**, due to the strong orbit overlap (covalent bonds) between metal and 1L-TMD atoms. In particular, ρ_{min} in Au-MoS_2 (**Figure 50c,d**)] and In-1L-TMD edge contacts are significantly increased compared to that of their top contacts (**Figure 44a,b,g**), indicating a decrease in resistance by changing contact configurations from top contacts into combined contacts (**Figure 24c**). Low contact resistance of combined-contact configuration has been demonstrated on Au-MoS_2 **[23]**, Ti-MoS_2 **[5]** and In-WSe_2 **[7]** contacts via experiments.

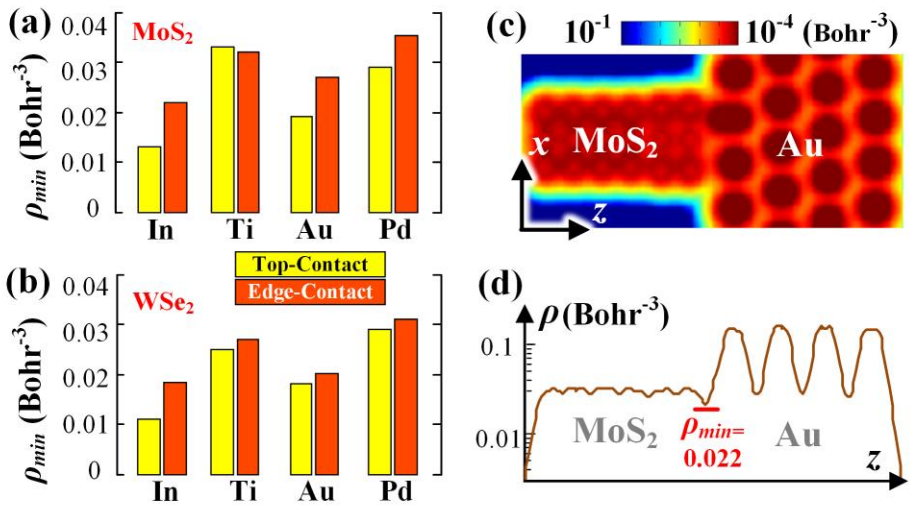


Figure 50: Electron density of top and edge contacts.

(a),(b) Minimum of average electron density values in the x-y plane in Fig. 18(a) at the interfaces for all top and edge contacts. Ti, Pd, Mo, and W may form better top contacts due to higher interface electron density. Electron densities are significantly increased for edge contacts. (c),(d) Valence electron densities of Au-MoS_2 edge contact. (c) Average density along y projected on the x-z plane; (d) average density in the x-y planes normal to the z axis. The red number in (d) indicates the minimum electron density at the interface.

Furthermore, the electron localization functions (ELF, a function of the 3D coordinates, which is large in the regions where orbitals localize **[247]**) for Au-MoS_2 top and edge contacts are calculated and shown in **Figure 51**. Because orbital overlaps between metal and 1L-TMD atoms are more efficient in edge contacts, the ELF at the metal-1L-TMD interface is much higher at the interface in edge contacts (**Figure 51d**) than that of top contacts (**Figure 51b**). In other words, strong covalent bonds are formed in edge contacts, indicated by green dashed curves in **Figure 51d**.

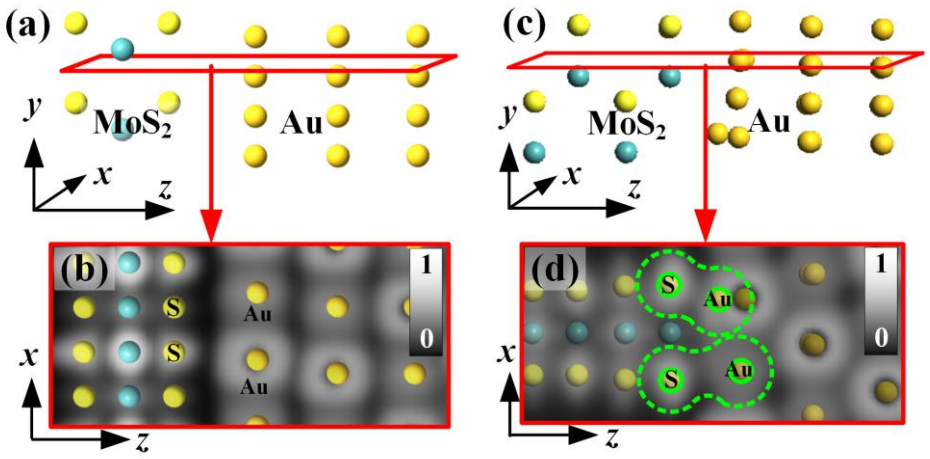


Figure 51: Electron localization functions of Au-MoS_2 top and edge contacts.

(a),(c) The cleaved x-z planes (red rectangles) used to show electron localization functions (ELF) for (a) Au-MoS_2 top contact and (c) Au-MoS_2 edge contact. (b),(d) ELF plots on the cleaved x-z plane in Au-MoS_2 (b) top contact, (d) edge contact. Half-transparent dots indicate positions of atoms. High ELF (closer to 1) indicates high probability of finding an electron. For edge contact, Au-MoS_2 has overlapping electron orbitals (Au-S bonds, indicated by green dashes) resulting in the increasing of electron density as shown in Figure 50. Thus, the contact resistance is reduced by using edge contacts.

The strong orbital overlaps, absence of SB, and lower tunnel barriers are all advantages of edge-contact configurations compared to top contacts. Hence, edge-contacted configurations have a higher capability of electron injection and thereby decrease the contact resistance. If contact dimensions are large (i.e., number of atoms across the contact area is much greater than those along the contact perimeter), top contacts have an advantage in terms of contact area. However, for a fixed number of 1L-TMD atoms contacted by metal,

the edge-contacted configuration is better than the top-contacted configuration. Hence, the combined contact (**Figure 24c**, combination of top contact and edge contact) is more desirable. It is worth noting that for multilayer TMD devices, due to process voids, the electrode metal may fail to contact all of the layers at the edges, and the gate electrode may not modulate all the layers due to screening. Therefore, the number of TMD layers should be optimized **[5]**.

2. Edge Contacts to Multilayer 2D Materials

Considering the large conductivity anisotropy of 2D materials between the in-plane and out-of-plane directions, edge-contacts are particularly relevant to multilayered 2D materials **[216]**. A model accounting for both top- and edge-contacts to multilayer graphene (MLG) **[215]** showed that in this case edge contacts significantly reduce the overall contact resistance **[216]**. Another model, based on a resistor network with consideration of back-gate screening effect **[248]** has been used to compare top-contacted and edge-contacted multilayer graphene devices. Using the model, the extracted edge-contact resistance from experiments is 150-360 $\Omega \cdot \mu m$ for each graphene layer, which is relatively small compared to the tunneling resistances between each layer **[248]**. Similar work has been reported **[249]**, where the currents flowing through the graphene surface and edges are theoretically and experimentally investigated by patterning of graphene under the contact metal with different perimeter-to-area ratio.

For multilayer TMD semiconductors, only the top layer can be hybridized by metal top-contacts, and thus only the vdW gap between the metal and top layer of TMD is eliminated, as predicted by DFT **[5], [6]**, and **Figure 52**, **Figure 53**. The vdW gaps between the bottom layers still exist.

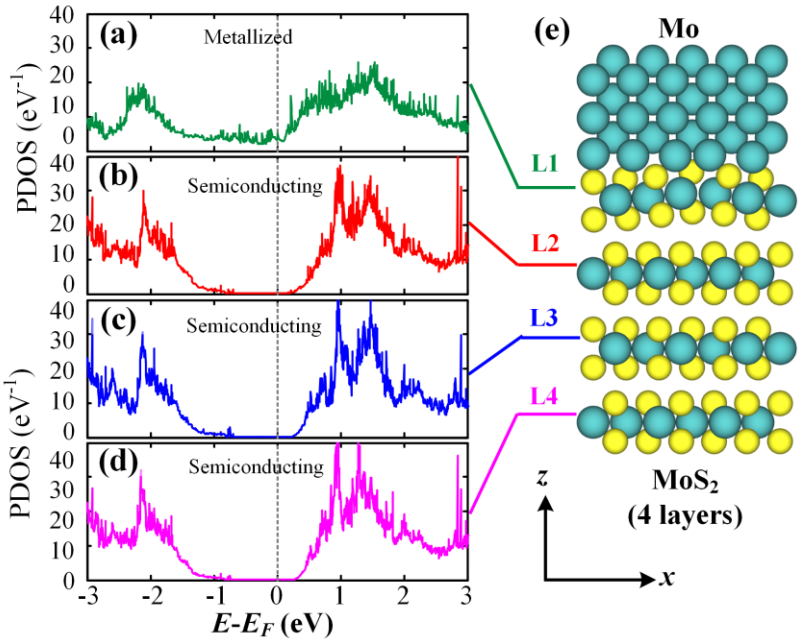


Figure 52: DFT simulation of Mo top contact to ML MoS_2.

(a-d) PDOS of the individual layers (from layer 1 (L1) to layer 4 (L4)) in a 4-layer MoS_2 film under Mo top-contact. (e) Optimized unit cell of top-contacted Mo-MoS_2 (4 layer) system in side view.

Figure 53a shows the relaxed contact regions at the interface between MoS_2 (3L) –Ti surface for DFT calculations. For a top contact (Ti contacting the top layer only), there is a high electron density (0.027 Å^{-3}) between the upper-most MoS_2 layer and Ti, while the electron density stays constant between MoS_2 layers (L1-L2 and L2-L3 in **Figure 53b**). The doping effect on the first MoS_2 layer is also confirmed from the PDOS (**Figure 53c, d**). After depositing Ti onto the first layer of MoS_2, its band gap vanishes due to the doping effect. However, L2 and L3 still have the band gap. Therefore, for a top contact (Ti contacting the top layer only), the DFT calculation (**Figure 53**) reveals that Ti solely influences the upper-most layer of MoS_2 leading to the experimentally observed performance degradation **[5]**.

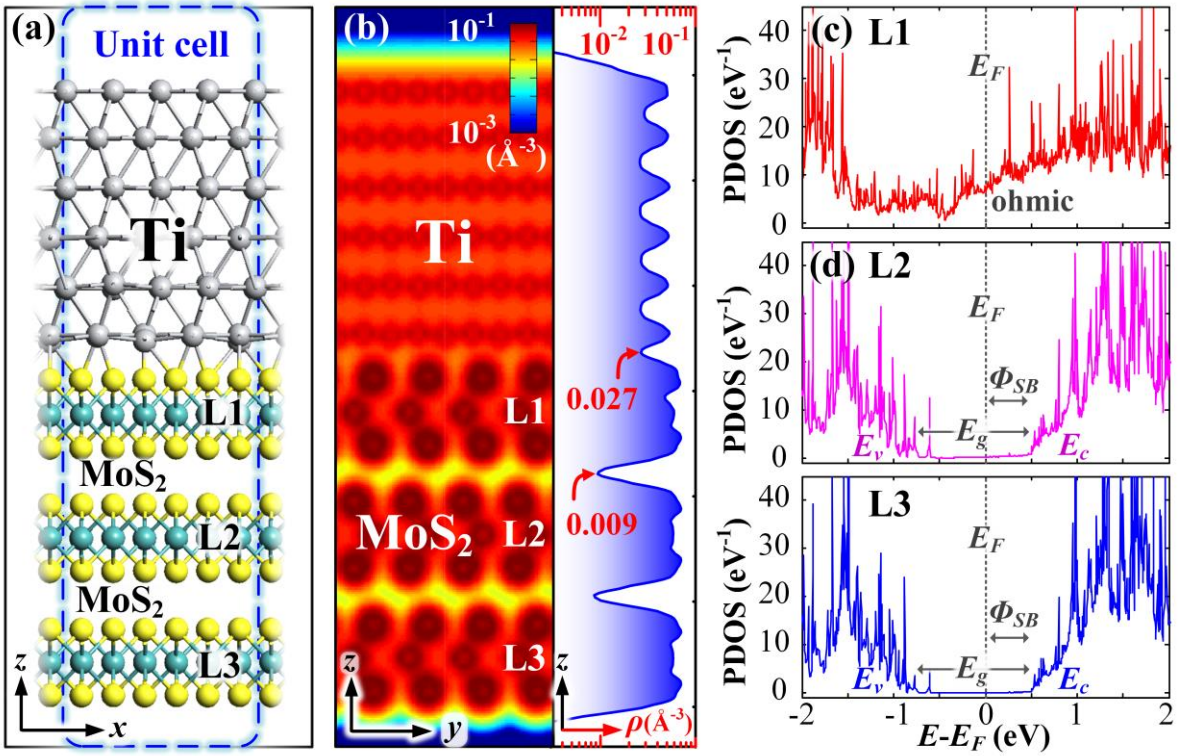


Figure 53: DFT simulation of Ti top contact to ML MoS_2.

(a) Side view of the relaxed contact regions at the interface between MoS_2 (3L)–Ti surface. (b) Contour plots of the average electron density. The contour plot represents the average electron density along the *x*-axis. Right hand side shows the plot of average electron density along the *x*-*y* plane corresponding to MoS_2 (3L) – Ti system. (c) Partial density of states (PDOS) of first layer (L1) (with Ti contact) MoS_2. (d) PDOS of second (L2) and third layer (L3) of MoS_2. Ti only influences the top layer (L1) of MoS_2 due to the formation of Ti-S bonds. The band gap of first layer (L1) MoS_2 vanishes after contact with Ti, while L2 and L3 still have large Schottky barriers (Φ_{SB}).

To achieve high current, most of the MoS_2 layers should connect to the contact metal from the side or edge (edge contact shown in **Figure 54a, b**). The DFT calculation (**Figure**

54c) shows that sulphur atoms can form strong covalent bonds with Ti atoms, which not only provide access to all available conducting channels but also reduces the $R_{contact}$.

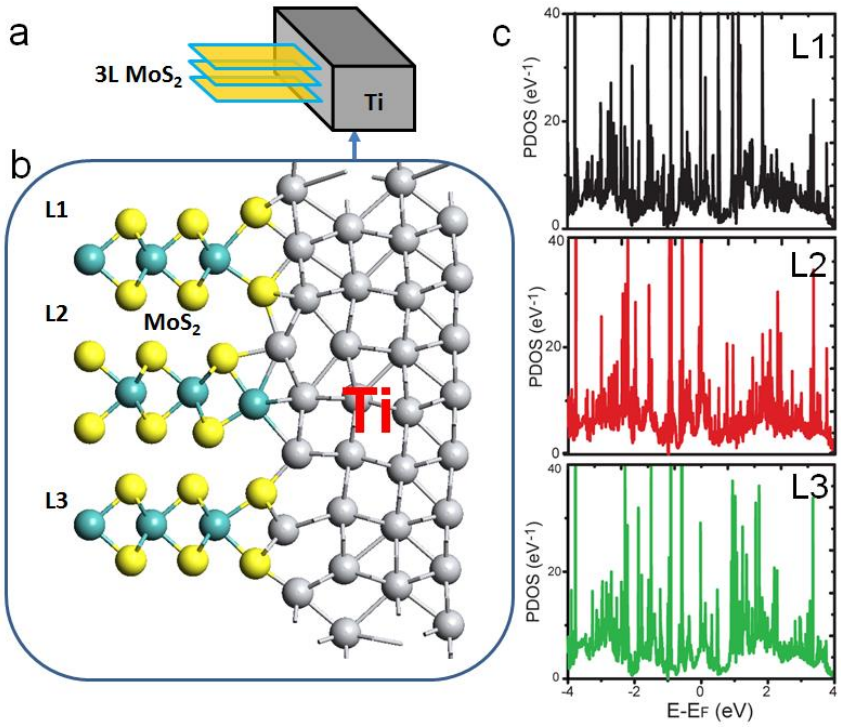


Figure 54: DFT simulation of Ti edge contact to ML MoS_2.

(a) Schematic view of an edge contact. (b) Side view of the relaxed contact regions at the interface between MoS_2 (3L) -Ti. (c) PDOS of each layer of MoS_2 with Ti (L1, L2, L3 from top to bottom). Sulfur atoms can form strong covalent bonds with Ti, hence the MoS_2 (edge-contacted) loses its band gap, which is reflected by the PDOS plots of the three MoS_2 layers shown in (c), indicating an ohmic contact.

Hence, in order to improve the carrier injection to the bottom layers, edge contacts to all the layers are preferred. This will also be pointed out later by experimental comparison of devices on various layers in the next section.

E. Demonstrated Contacts in Field-Effect Transistors

1. Mo-Contacted MoS_2 FETs

Since Mo is one of the elements forming MoS_2, Mo has a great potential to form perfect interface with MoS_2. It has been shown by DFT calculation previously that Mo can indeed form *Type 3* contact to MoS_2 with an ultra-low *Schottky barrier* (*2*) height of 0.1 eV. Therefore, in this part, the feasibility of Mo as a high-performance contact metal to MoS_2 in monolayer and multilayer MoS_2 FETs will be explored. I demonstrate by experiments that high mobility and low contact resistance can indeed be achieved in Mo-contacted MoS_2 FETs, which is consistent with the DFT simulation results. Through this study, I also highlight that apart from choosing a proper work-function metal, the detailed physics of the interface between the metal and MoS_2 layers plays an important role, which should be adequately comprehended in order to achieve high performances in emerging MoS_2 FETs.

MoS_2 films (1-5 layers) are prepared by mechanical exfoliation of bulk MoS_2 (SPI Instrument Inc.) on 72 nm Al_2O_3/Si (highly n-doped) substrate, where a heavily n-doped Si is used as the back gate, as shown in **Figure 55**. We employed Secondary Ion Mass Spectrometry (SIMS) to measure the samples. Only very low concentrations of Cl and Se were detected. Hence, the sample is slightly n-doped and can provide representative results. The thicknesses of MoS_2 films are identified using the optical contrasts observed from optical microscope**[250], [251]** as well as height measurement data from Atomic Force Microscope (AFM) (**Figure 56**). The source and drain regions are defined by electron-beam lithography followed by a metal deposition of Mo (10 nm) followed by Au (100 nm). Annealing is performed at 420 K for 2 hours in order to remove any absorbed moisture and solvent molecules and also improve the adhesion of contacts.

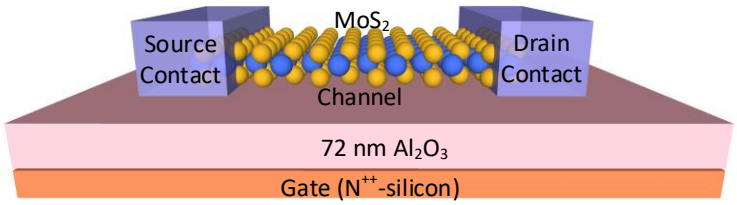


Figure 55: A typical topology of a back-gated MoS_2 FET.

The SEM images of the fabricated back-gated FET devices are shown in **Figure 56**. In this study, all measurements are performed in vacuum (1×10^{-6} mbar) at room temperature. For four-point-measurements (**Figure 56b**), current flows from V1 to V2. Simultaneously, voltages are measured on V3 and V4.

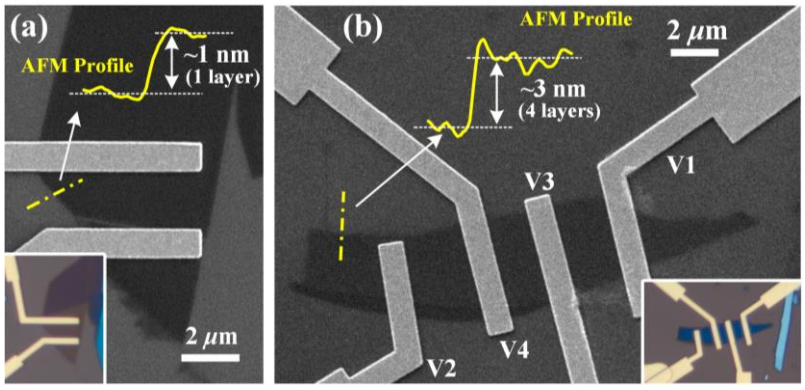


Figure 56: SEM micrographs of Mo-MoS_2 FETs.

(a) Monolayer and (b) 4-layer MoS_2. Inner figures are optical microscopic images showing the contrast of different sample thicknesses. Yellow dotted lines indicate paths of AFM measurement. Yellow curves show AFM profiles (noise level: ±0.25 nm).

Figure 57a shows the transfer characteristics curves (drain-source current I_{ds} vs. back-gate voltage V_{bg}) of the back-gated MoS_2 FETs with Mo (10 nm) /Au (100 nm) Source/Drain contacts, for channel thickness of 1-layer and 4-layers, respectively. The curves clearly display an n-type behavior with ON/OFF ratios exceeding 10^3 at drain-source

voltage V_{ds}=0.1V.

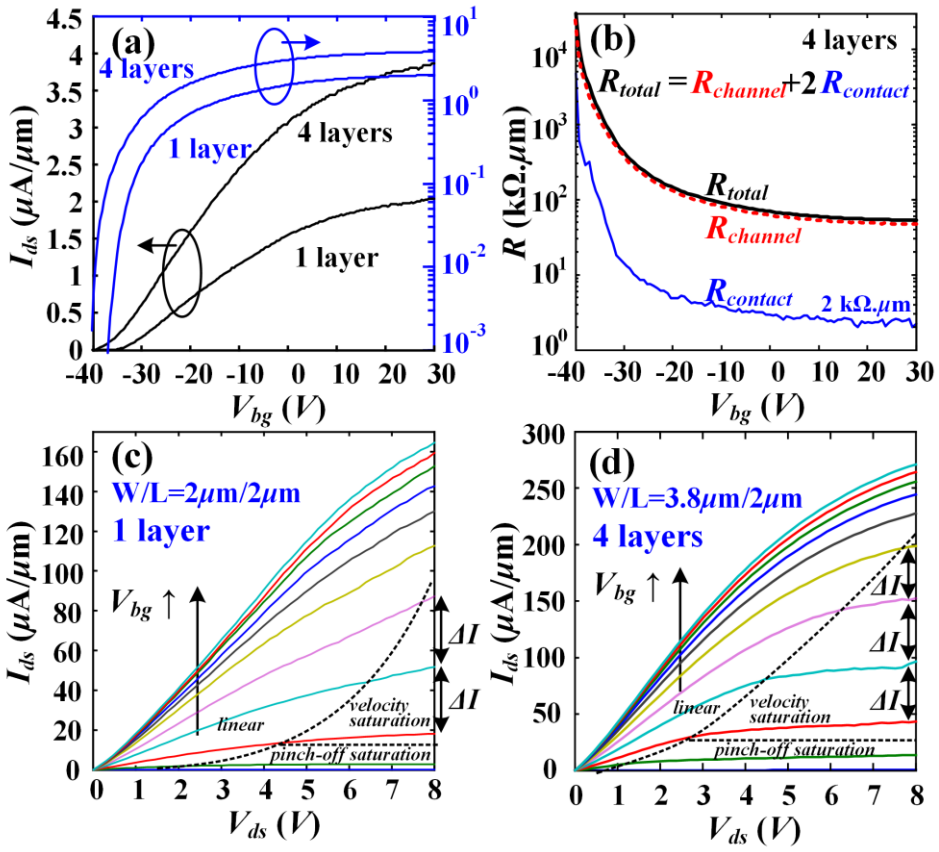


Figure 57: I-V characteristics of Mo-MoS_2 FETs.

(a) I_{ds}-V_{bg} curves (transfer characteristics) of monolayer and 4-layer MoS_2 back-gated FET with Mo contact, V_{ds}=0.01V. Black and blue curves denote linear and log scale plots, respectively. The *y*-axis in blue shows log scale values. (b) Contact resistance ($R_{contact}$), channel resistance ($R_{channel}$), and total resistance (R_{total}) as a function of back gate voltage (V_{bg}) for 4-layer MoS_2 FET. I_{ds} = 0.1 μA. (c, d) I_{ds}-V_{ds} curves (output characteristics) of (c) monolayer and (d) 4-layer MoS_2 back-gated FET with Mo contact. V_{bg} varies from -30 V to 30 V. The dotted curves separate the three operation regimes. The corresponding contact resistivity is 2.2×10^{-5} Ω cm^2.

It is difficult to make transmission line measurements on such nano-crystals with limited length or area. Hence, we employed four probe measurement and roughly estimated the contact resistance by subtracting the channel resistance ($R_{channel}$) from the total resistance (R_{total}) **[213], [252]**. For the 4-layer sample, $R_{channel}$ is denoted by the red curve in **Figure 57b**. The channel resistance is estimated using the dimensions of the channel regions and the resistivity measured using probes V3 and V4 (**Figure 56b**). Black curve in **Figure 57b** corresponds to R_{total} measured between V1 and V2 (**Figure 56b**).

For evaluating contacts to MoS_2, contact resistance (resistance × width) rather than contact resistivity (resistance × area) is used in this work in order to make fair comparisons with other works **[92]**, which is more conventional for 2D materials. The contact resistance ($R_{contact}$, blue curve in **Figure 57b**) can be extracted by subtracting the $R_{channel}$ from R_{total} and a value of $R_{contact} \approx 2$ kΩ.μm is found at V_{bg}=30 V. This value is 1-2 decade lower compared to that of Ti contact on multilayer MoS_2 in others' works (≈80 kΩ.μm **[39]** and ≈150 kΩ.μm**[253]**). It is also more than one half lower compared to that of Ni/Au contact to multilayer MoS_2 at V_{bg}=50 V (4.5 kΩ.μm) **[92]** and similar with Ti contact to few layer MoS_2 (≈3 kΩ.μm and ≈1.6 kΩ.μm for 4- and 5-layers, respectively) in our recent work **[5]**. Moreover, this $R_{contact}$ can be further minimized at higher I_{ds} or V_{bg}.

Figure 57c and **d** show the output characteristics (drain-source current I_{ds} vs. drain-source voltage V_{ds}) of the monolayer and 4-layer MoS_2 FETs, respectively. Both of the I_{ds}-V_{ds} curves display a slightly non-linear behavior, indicating that the contact is a slightly Schottky contact. This result is consistent with the simulation prediction of Schottky barrier = 0.13 eV in the previous sections. Meanwhile large ON-currents are observed in back-gated Mo-MoS_2 FETs with various thicknesses, as summarized in **Table 6**.

Table 6: Mobility and ON current (I_{ON}) of back-gated Mo-MoS_2 FETs.

# of MoS_2 layers		1	2	3	4	5
Back-gated FET Mobility ($cm^2/V.s$)	V_{ds}= 0.1V	~11	~11	~27	~22	~25
	V_{ds}= 1 V	~13	~14	~27	~26	~26
Back-gated I_{ON} (μA/μm) V_{bg}= 30 V	V_{ds}= 1 V	18	27	30	42	34
	V_{ds}= 8 V	165	183	201	271	204

In addition, slight current saturation can be observed in **Figure 57c** and **d** at high V_{ds}, which can improve the noise margins and hence, is important for digital circuit applications. Note that the effective drain-source voltage, effective gate-source voltage and the threshold voltage can be denoted as V_{ds_eff} (= V_{gs} - $2R_{contact}$ I_{ds}), V_{gs_eff} (= V_{gs} - $R_{contact}$ I_{ds}), and V_{th}, respectively. We can then observe that in most parts of the saturation regions in **Figure 57c** and **d**, the voltages do not satisfy pinch-off saturation condition, $V_{ds\_eff} > V_{gs\_eff} - V_{th}$, which indicates that the devices are mostly operating in velocity saturation regime ($V_{ds\_eff} > V_{sat}$ and $V_{gs\_eff} - V_{th} > V_{sat}$, where V_{sat} is the saturation voltage). The velocity saturation can also be confirmed by the linear increment of I_{ds} vs. V_{bg} (shown by ΔI in **Figure 57c** and **d**), according to CMOS theory.

Moreover, in the multilayer device, due to the lower source/drain contact resistance, the V_{gs_eff} and V_{ds_eff} values are increased and hence, more prominent current saturation can be observed in the multilayer device, as can be observed by comparing **Figure 57c** and **d**.

We can also estimate the effect of contact resistance on the FET mobility extracted through two-terminal measurements. The mobility is extracted using the well-known equation: $\mu=(L/W)g_m C_{ox}^{-1}$ without deducting the contact resistance. **Table 6** lists the mobilities of Mo-MoS_2 FETs with various thicknesses (1-5 layers) measured at V_{ds} = 0.1 V and 1 V without deducting $R_{contact}$. For a thick MoS_2 flake, Mo-MoS_2 contact is expected to

provide lower $R_{contact}$ due to its multiple conducting channels. This is apparent in the range of 1 to 4 layers, as shown by the I_{ON} and mobilities in **Table 6**. However, this trend stops at 4-5 layers, due to the fact that the electrode metal may fail to contact all the layers, indicating that edge-contacts to every layer are important for achieving low resistance multilayer 2D materials based semiconducting channels **[1]**. In addition, V_{bg} cannot modulate the top layers due to the V_{bg} screening (in back-gated devices), thereby resulting in a high $R_{contact}$. That is to say, to achieve high current and low $R_{contact}$, all the layers in the MoS_2 channel should connect to the contact metal from the edges, which in agreement with both theoretical calculations **[1]** and experiments **[7]**.

As pointed out earlier by simulation, though Mo contacts form lower Schottky barrier with MoS_2, the PDOS near Fermi level is limited (**Figure 39**). Overall, compared with Ti contacts in the next section, Mo contacts provide compatible ON-current (1-4 layer MoS_2), improved FET mobility (1-4 layer MoS_2) and reduced contact resistance (4-layer MoS_2). Considering the better chemical stability and superior thermal and electrical conductances (1.38 W/cm.K and 0.187×10^6 /cm.Ω, respectively) of Mo, it can be a more promising contact metal for MoS_2 compared to Ti.

In conclusion, this section reports high-performance 1-5 layer MoS_2 FETs with low contact resistance using Mo as the contact metal. Few-layer (~ 4 layers) MoS_2 FETs with Mo contacts show better potential for high-performance digital circuits due to their small contact resistances (~2 kΩ.μm), high ON-currents (271 μA/μm at V_{ds}= 8 V) and high mobilities (~27 cm^2/V.s). The results obtained in this study not only reveal an alternative contact metal to Ti for emerging MoS_2 FETs, but also highlight the unique nature of metal-2D contacts ─ wherein the properties of contacts strongly depend on the degree of atomic orbital overlapping at the interfaces and cannot be intuitively predicted by solely considering

work function values and Schottky theory.

2. Ti-Contacted MoS_2 FETs

According to **Section C.6**, 1L MoS_2 FET with Ti contact should a Schottky barrier of 0.35 eV. Using the thermionic emission equation for 2D materials, the Schottky barrier between MoS_2 and Ti can be accurately extracted. In one of my works **[42]**, the extracted Schottky barrier between monolayer MoS_2 and Ti varies from 0.3–0.35 eV measured from 6 monolayer devices, which is a good match with the calculation in **Section C.6**.

The Schottky barrier between monolayer MoS_2 and Ti is significantly larger than the Schottky barrier between multilayer MoS_2 (bandgap: 1.2 eV) and Ti, which is around 50 meV **[91]**. Considering the large bandgap of monolayer MoS_2 (1.8 eV), the extracted Schottky barrier between monolayer MoS_2 and Ti is quite reasonable given that monolayer MoS_2 has smaller electron affinity than multilayer.

To study the contact effect on the performance of MoS_2 FET, it is desirable to extract the contact resistance. Four-terminal-measurements method is employed to extract the contact resistance (R_c) at various V_{bg}. By injecting a constant current (I_{ds}) into the four-terminal configuration, $R_{channel}$ (between the inner two electrodes) can be directly measured. Then, R_{total} between the inner two electrodes is measured using two-terminal-measurements by applying the same current employed in four-terminal-measurements. Hence, R_c can be extracted by subtracting the $R_{channel}$ from R_{total}.

Figure 58a is the contour plot of R_c as function of V_{bg} and I_{ds} applied for the four-terminal -measurements. It is found that R_c is dependent on the values of applied I_{ds} as well as the V_{bg} as shown in **Figure 58a**. At small I_{ds} (below 20 µA) R_C shows strong V_{bg} dependence, in which R_c is ~25 kΩ.µm at V_{bg}= -5 V, while R_c can be reduced to 7 kΩ.µm at high V_{bg} (30 V). When I_{ds}>40 µA, R_c is significantly reduced at low V_{bg} and shows less V_{bg}

dependence.

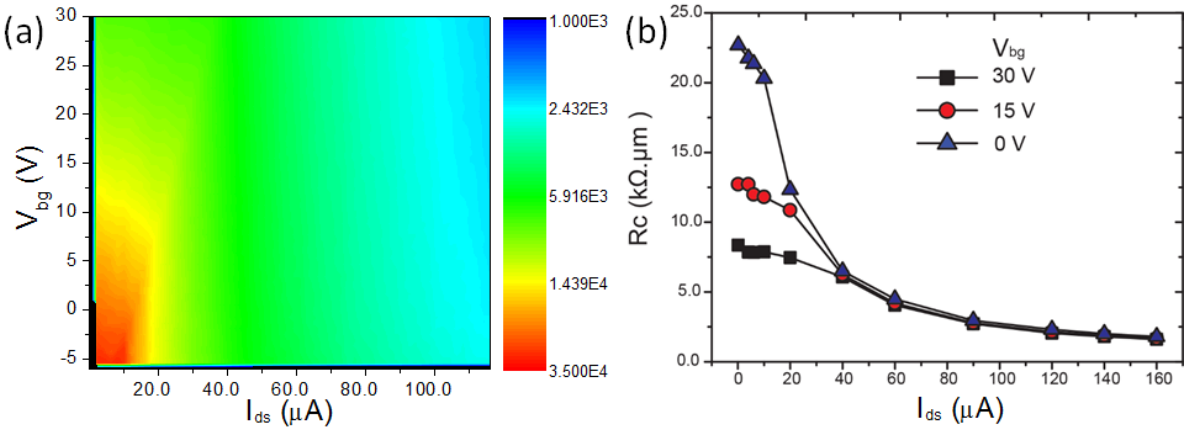


Figure 58. Contact resistance R_c of 1L-MoS_2 FET.

(a) Contour plot of R_c as function of V_{bg} and I_{ds} used for the 4-point measurements. (b) R_c as a function of I_{ds} at various V_{bg}.

Various R_C as a function of I_{ds} at V_{bg}= 0, 15, and 30 V are also plotted in **Figure 58b**. At low I_{ds} (<40 μA), R_c shows strong V_{bg} dependence, implying that Schottky barrier is mainly tuned by the gate electrostatics. However, when I_{ds}>40 μA, R_c has less dependence on the $V_{bg,}$ indicating that the amount of electrons injected from source is much larger than the electrons generated by gate electrostatics. Hence, the large amount of electrons injected from source can heavily dope monolayer MoS_2 resulting in a very narrow Schottky barrier. The minimum extracted R_c is ~1.3 kΩ.μm (I_{ds}=150 μA, V_{bg}=30 V), which is much smaller than any reported value on metal contact with monolayer MoS_2.

Compared with 1L MoS_2, FL MoS_2 flakes (defined as several nm to sub-10 nm in this work), have a higher DOS than that of 1L MoS_2, a lower bandgap and thus lower Schottky barrier height, which can potentially lower contact resistance and carry higher current. Moreover, FL MoS_2 flakes retain the capability of overcoming short channel effects. Hence,

it is desirable to study FL MoS_2 FET devices to maximize performance of future MoS_2 devices.

In another work of mine **[5]**, R_c of 1L MoS_2 FET with Ti contact is found to be around 740 kΩ.μm at V_{bg}=30 V, while the 15L MoS_2 FET exhibits a record low R_c of ~0.8 kΩ.μm when V_{bg}> -4 V. This record low R_c is close to the metal-silicon contacts in CMOS technology **[50]**, and represents a major advancement from current state-of-the-art MoS_2 transistors. Compared to FL MoS_2 FETs with Au/Ni contact (4-17 kΩ.μm) **[92]**, FL MoS_2 FET with Ti contacts exhibits a smaller $R_{contact}$ that shows a smaller dependence on applied V_{bg}, indicating that Ti forms better contact with FL MoS_2 than that of Au/Ni. The lower dependence of $R_{contact}$ on V_{bg} (when V_{bg} is above a certain value) also reflects that Ti can heavily dope MoS_2, thereby resulting in a good contact, which has also been confirmed by theoretical predictions in previous sections.

The $R_{contact}$ of both 1L and 15L MoS_2 decreases with increase of temperature due to enhanced thermionic emission over the Schottky barrier. At high temperatures, electrons can occupy higher energy levels leading to more electrons flowing over the Schottky barrier and contributing to the current injection, thereby reducing the contact resistance. However, when temperature is above 300 K, $R_{contact}$ of 15L MoS_2 exhibits much smaller change (~0.2 kΩ.μm) than that of 1L MoS_2 (~30 kΩ.μm), indicating that thermionic emission has lower impact on 15L MoS_2-Ti contact. This implies that the Schottky barrier of 15L MoS_2-Ti contact is much smaller and thinner than that of 1L MoS_2-Ti contact. Therefore, FL MoS_2-Ti devices enable better contacts, in which tunneling through the Schottky barrier dominates the drive current due to the small and thin barrier.

In addition, for FL MoS_2 devices, good edge contacts can significantly enhance device performance. The benefit of making good edge contacts is demonstrated by a top-gated FL

MoS_2 FET that exhibit high ON current (24 $\mu A/\mu m$ for 5 nm MoS_2) even without source/drain doping **[5]**. As summarized in **Table 7**, few-layer (5L-15L) MoS_2 FETs show better potential for high performance digital circuits due to their small contact resistances and high mobilities.

Table 7. $R_{contact}$, intrinsic mobility of MoS_2 FETs with various thicknesses.

SiO_2 (90 nm)/Si substrates were used. 1L, 2L, 5L and 8L MoS_2 FETs have Ti (10 nm)/Au (100 nm) contacts, while 15L and 46L MoS_2 FETs have Ti (50 nm)/Au (100 nm) contacts. Mobility is calculated from *channel conductance* (measured by four-point-measurements)-V_{bg} plots at V_{ds}= 0.01 V and V_{bg} is swept from -30 V to 30 V.

Layer #	1L	2L	5L	8L	15L	46L
$R_{contact}$ (KΩ.μm)	740	15.6	1.56	1.24	0.**78**	53
Mobility (cm^2/V.s)	~13	~21	~52	~**54**	~47	~19
Top gate I_{ON} (μA/μm) V_{ds}=1V	1.2 V_{tg}=0V	N/A	N/A	**24** V_{tg}= -2.2V	N/A	N/A
Back gate I_{ON} (μA/μm) V_{ds}=1V, V_{bg}=30V	10	20	**46**	40	30	6.7

Note that back-gated devics have higher I_{ON} than top-gated devices, which can be attributed to the fact that back gate voltage always modulates the Schottky barrier at S/D regions, while top gate voltages can not thin the Schottky barrier due to the device geometry (Fig.11a) of top-gated devices.

3. 1L WSe_2 n-FETs

In comparison to the widely studied monolayer MoS_2, studies focusing on monolayer WSe_2 are fewer. As a semiconductor material, bulk WSe_2 possesses good stability, and is more resistant to oxidation in humid environments than sulphides **[254]**. Bulk WSe_2 crystal

devices have been studied with mobilities as high as 500 cm^2/Vs **[255]** (extracted after deducting contact resistance) exhibiting the excellent potential of WSe_2 for device applications.

Experimental **[25]** work have shown that monolayer WSe_2 is the first TMD material in which p-type conducting behavior is observed by using high work function metal (Pd) as the contact (achieving a high FET hole mobility of around 250 cm^2/Vs). This important property of monolayer WSe_2 provides a promising possibility to design and fabricate complementary digital logic circuits on the same monolayer WSe_2 film if high-performance n-type monolayer WSe_2 device can be simultaneously achieved by selecting the proper contact metal. However, contact resistance has been found to be a key factor that can significantly influence device performance of bulk WSe_2 FETs (extracted mobility is 100 $cm^2/V.s$ without contact corrections) **[255]** and monolayer WSe_2 FETs **[25]**.

Hence, it is necessary to explore the metal contacts to monolayer WSe_2 to achieve high performance n-type WSe_2 FETs. My theoretical work in **Section C.6** has shown that it is possible to form n-type ohmic contact to monolayer WSe_2 by suitable contact metals, thereby providing guidance to experimental selection and exploration of metal-WSe_2 contacts for achieving high performance n-type WSe_2 FETs. Using Indium as contacts, high-performance n-type monolayer WSe_2 back-gated FETs (**Figure 59**) are demonstrated by us **[7]** with a record ON-current of 210 $\mu A/\mu m$ at V_{ds}=3 V and I_{ON}/I_{OFF} $>10^6$, with a record electron mobility of 142 cm^2/Vs. The electron mobility is further enhanced to 202 $cm^2/V.s$ on a back-gated device with I_{ON}/ I_{OFF} $>10^6$ and ON-current of 205 $\mu A/\mu m$ at V_{ds}=3 V by depositing a high-κ dielectric (Al_2O_3) layer over the channel region of the WSe_2 FET.

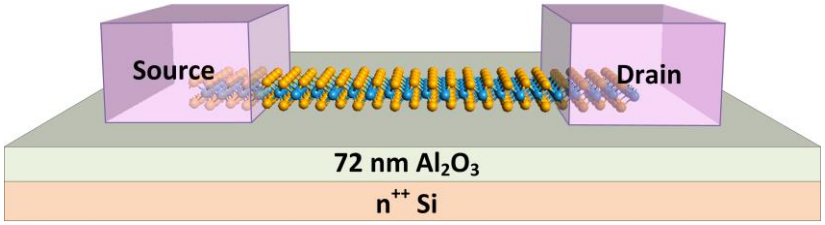


Figure 59: Schematic of back-gated WSe_2 monolayer FET.

Highly n-doped silicon serves as back gate.

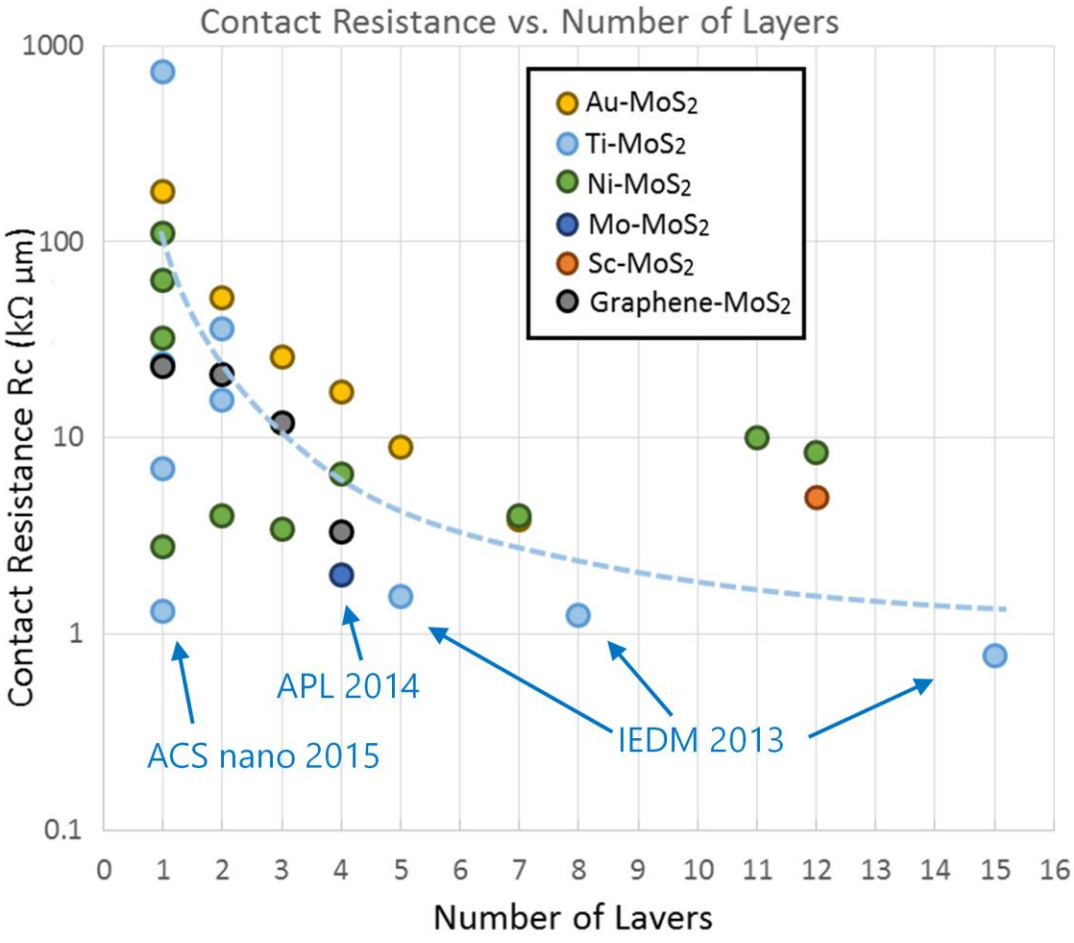


Figure 60: Comparisons of our metal-MoS_2 contacts with others works.

Note that this plot is dated till 2015, when our three works dominate the contact resistance records.

4. Record Low Contact Resistance

As shown in **Figure 60**, three of my demonstrated experimental works on contact resistance (IEDM 2013 **[5]**, APL 2014 **[6]**, ACS nano 2015 **[42]**) are compared with literature. All the three works report the record low contact resistance by the years of their publications.

F. Seamless Contacts

Apart from 3D metals, one must also consider the possibility of contacting 2D semiconductors using other (or the same) low-dimensional materials. "Native" chemical bonds are expected at such interfaces.

For example, because there are both metallic allotropes (metallic CNTs, graphene and wide graphene ribbons, etc.) and semiconducting allotropes/structures (semiconducting CNTs, graphene nanoribbons (GNRs), vertically biased AB-stacked bilayer graphene, etc.) in the carbon family, one can first fabricate semiconducting (or metallic) carbon and then tune one side to be metallic (or semiconducting). Relevant theoretical studies include CNT-graphene interface (**Figure 61a**) **[256]**, graphene-GNR interface (**Figure 61b**) **[3], [256]** and monolayer-multilayer graphene interface **[257]**, etc. The bonds at those interfaces are native sp^2 carbon-carbon bonds, same as the bonds inside both on the metallic and the semiconducting side, resulting in a "seamless" contact between the two sides.

In the next section and **[3]**, an all-graphene circuit scheme based on "seamless" contacts was proposed and evaluated by numerical simulation. The reported "seamless" contacts, where both contacts/interconnects (wide graphene) and transistors (GNRs) are envisioned to start from a single sheet of graphene, greatly reduced the contact resistance (down to 0.1

kΩ·μm) and improved the circuit performance including noise margin, speed and power consumptions.

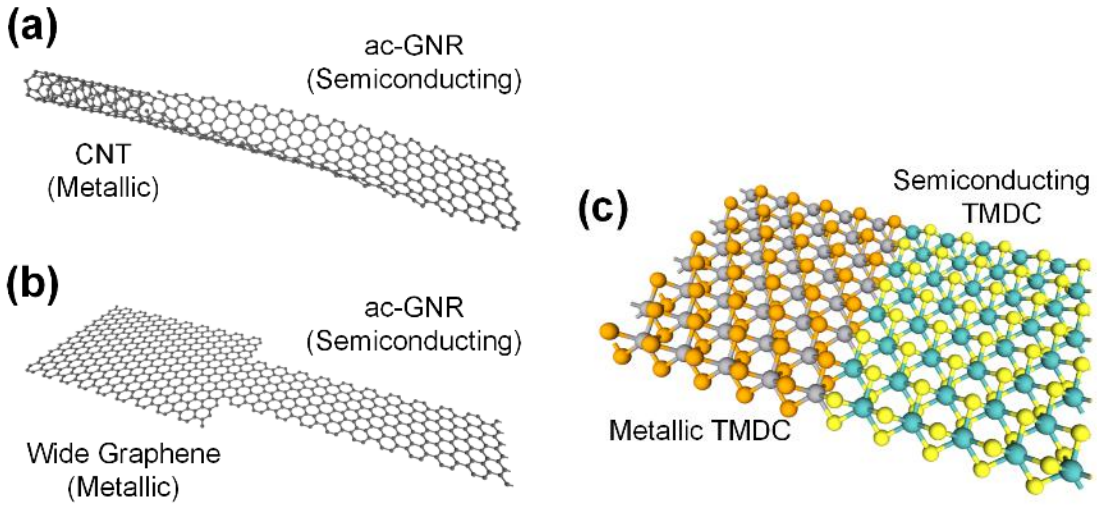


Figure 61: Various "seamless" contact schemes.

(a) CNT-GNR contact; (b) Graphene-GNR contact; (c) Metallic TMD-Semiconducting TMD contact.

The concept of "seamless" contacts from such all-graphene circuits can also be adapted to other 2D semiconductors (**Figure 61c**). In recent studies **[258], [259]**, contacts between 1T-MoS_2 (metallic) and 2H-MoS_2 (semiconducting) have been fabricated using phase engineering **[258], [260]** (changing 2H phase into 1T phase). The resulting contact resistance of 0.2 kΩ·μm is the lowest ever reported for this material. Another option would be to grow metallic and semiconducting TMDs in sequence in a single CVD process. Further theoretical studies are needed for this "seamless" contact scheme on 2D materials other than graphene.

G. All-Graphene Monolithic Logic Circuits

This section introduces and explores an "all-graphene" device-interconnect co-design scheme, where a single 2-dimensional sheet of monolayer graphene is proposed to be monolithically patterned to form both active devices (graphene nanoribbon tunnel-field-effect-transistors) as well as interconnects in a seamless manner. **[3]** Thereby, the use of external contacts is alleviated, resulting in substantial reduction in contact parasitics. Calculations based on tight-binding theory and Non-Equilibrium Green's Function formalism solved self-consistently with Poisson's equation are used to analyze the intricate properties of the proposed structure. It is shown that all-graphene circuits can surpass the static performances of the 22 nm complementary metal-oxide-semiconductor devices, including minimum operable supply voltage, static noise margin and power consumption.

1. Introduction

Graphene-based electronics has drawn tremendous attention since its discovery in 2004 **[88]**. Graphene is the first thermodynamically stable two-dimensional (2D) material that is composed of a single layer of carbon atoms arranged in a hexagonal lattice (**Figure 62a**) with zero bandgap (E_g) (**Figure 62b**). Lithographically narrowed graphene (graphene nanoribbon (GNR)) exhibits high potential for building energy efficient devices such as GNR tunneling field effect transistors (GNR-TFETs) **[261]–[263]** because of its direct E_g (**Figure 62c**) and unique E_g tunability property via lithographic control of its width **[57], [61], [264]–[266]**. Graphene has also been proposed as a potential candidate to replace copper for next-generation global interconnects due to its patternability and current-carrying capacity **[57], [59], [61], [267]**. While separate analysis of GNR-based devices and graphene interconnects have been reported in the literature **[57], [59], [61], [261]–[267]**, the real benefits can be harvested through an integrated device-interconnect co-design scheme.

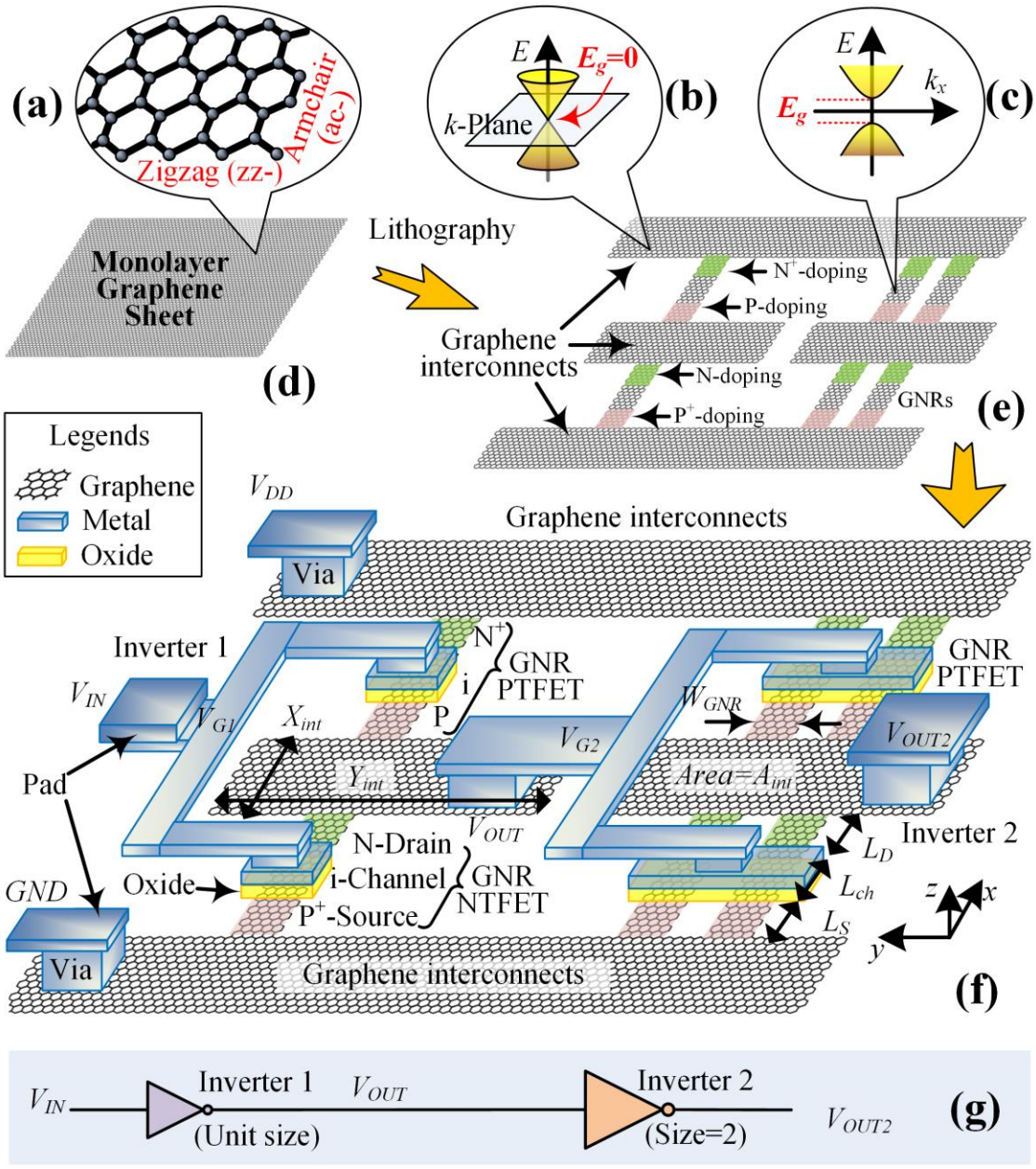


Figure 62. Concept of "all-graphene" monolithic logic circuits.

(a) The atomic structure of graphene. Armchair (ac) and zigzag (zz) are two different chiralities; (b) band structure of graphene and (c) band structure of armchair-GNR (ac-GNR);

(d-f) Schematics showing proposed fabrication steps of an "all-graphene" circuit (inverter chain): (d) monolayer graphene sheet; (e) graphene interconnects and GNRs patterned by lithography; source and drain regions are doped; (f) all-graphene circuit after deposition and patterning of metal and oxide;

(g) Circuit schematic of (f). Inverter 2 is double-sized using two GNR channels (hence fan out of Inverter 1 = 2).

Hence, the prospects of "all-graphene" circuits (**Figure 62d-f**) are explored and evaluated. In such design scheme, both devices (based on GNR-TFETs) and interconnects (based on wider graphene ribbons) are proposed to be concurrently fabricated by monolithically patterning a single sheet of graphene, thereby significantly simplifying the fabrication process. Moreover, this scheme of circuit design does not require local interconnects made of a different material to connect the devices within logic gates. Hence, the proposed "all-graphene" circuit can lead to substantial reduction in contact resistance and could potentially open up exciting prospects for designing ultra- dense and thin integrated circuits with unprecedented performance and energy- efficiency, and subsequently higher reliability. It is to be noted that this work is based on a paradigm integrating GNR-TFETs and graphene interconnects on a single layer graphene and is not to be confused with a previous work, which reported a circuit where graphene FET and metal-based inductors were integrated **[268]** using local metal interconnects and hence, cannot offer the unique advantages of the proposed "all-graphene" circuit.

2. Proposal of "All-Graphene" Circuits

Figure 62d-f show an all-graphene inverter chain design together with its proposed fabrication process in 3 steps: (d) synthesis of monolayer graphene sheet; (e) patterning of

the uniform graphene sheet and doping of GNRs to realize graphene interconnects and GNR devices; (f) depositing and patterning of gate oxide, gate metal, isolation oxide, via, pads and external interconnects.

The recent demonstration of graphene patterning down to sub-10 nm dimensions with atomically smooth edges via both top-down **[269], [270]** and bottom up **[175], [178]** processes lend sufficient credibility to the feasibility of such approach. It is worth noting that tight-binding (TB) approach provide consistent accuracy for band structure of armchair-GNR (ac-GNR, chirality shown in **Figure 62a**). Hence, the simulations in this work were performed with the assumption of smooth ac-GNR edges. Such E_g modulation for zz-GNRs is also observed in experiments for sub-10 nm widths, and hence, this work can be extended to any chiralities.

The doping of GNRs can be achieved by chemical doping (via edge doping **[271]**, intercalation doping **[267]** and substitution **[272]**), substrate doping **[273]** and electrostatic doping **[274]**, of which substrate and electrostatic methods are more controllable in small GNR areas. Hence, in this work, doping is considered to provide uniform charges in source and drain regions and quantified as Fermi potential ($|e\Phi_P|$ and $|e\Phi_N|$), defined as the energy difference between midgap energy E_i and Fermi level E_F (will be shown later, in **Figure 63b**).

Note that the widths of the channel regions in n- and p-type devices are made equal in order to obtain the same E_g. Hence, the sizing of all-graphene circuits is achieved by using multiple GNR channels, as shown in the multi-channel GNR-TFETs in Inverter 2 (**Figure 62f, g**). Because of the bipolar behavior of TFETs (electron-hole duality **[46]**), n- and p-type TFETs have almost the same tunneling currents, thereby n- and p-type devices can be made with identical sizing (unlike CMOS).

3. Design of "All-Graphene" Circuits

To understand of the transport across various wide-narrow graphene interfaces and GNR-TFETs, Non-Equilibrium Green's Function (NEGF) formalism **[275]** along with TB modeling of graphene/GNR band structures is employed. Self-consistent solution of Poisson's equation (PE) and NEGF is used to accurately account for the electrostatics. Transports in GNR-TFETs, interconnects and interfaces are solved separately in different NEGF modules (real space **[276]** for interconnects and interfaces and mode space **[277]** for GNR-TFETs) in self-consistent NEGF-PE iteration loops. Subsequently circuit performances are evaluated based on the lookup tables from the simulation results. Comparisons are then made with 22-nm CMOS high-performance (HP) and low-power (LP) models **[278]**.

At first, the active devices (TFETs) in the all-graphene circuit are designed. The GNR-TFETs are essentially reverse biased $P^{(+)}$-i-$N^{(+)}$ and $N^{(+)}$-i-$P^{(+)}$ type source-channel-drain structures where the source and drain regions are doped while the gate-controlled channel remains intrinsic. GNR-TFETs with symmetrically doped source and drain exhibit ambipolarity (remain ON for both high and low gate voltages (V_G, or V_{GS} if source is grounded)), which is detrimental for some circuit applications. Asymmetric (unequal) doping in source and drain of GNR-TFET **[277]** can be used to reduce ambipolarity. Hence, in this work, the n-type TFETs (NTFETs) with P^+-i-N doping and p-type TFETs (PTFETs) with N^+-i-P doping are used. The structure of such a NTFET is illustrated in the inset of **Figure 63a**. The output characteristics (V_{GS}-I_{DS} curve) of the NTFET (blue) is plotted in **Figure 63a** and compared with that of a symmetrically doped GNR-TFET (red). The TFETs consist of ac-GNR with N_W=40 (width of GNR W_{GNR} = 5 nm), E_g = 0.29 eV, channel length L_{ch} = 22 nm and single gate with 1.2 nm-thick HfO_2. Gate leakage is ignored. Drain to

source bias is V_{DS} = 0.2 V. Asymmetric doping induces an OFF state around V_{GS}~0. Doping is $|e\Phi_P|$ = 0.24 eV and $|e\Phi_N|$ = 0.11 eV. I_{ON}/I_{OFF} for P⁺-i-N is 1.6×10^3. The band diagrams in various regions of input characteristics are shown schematically in **Figure 63b-d**.

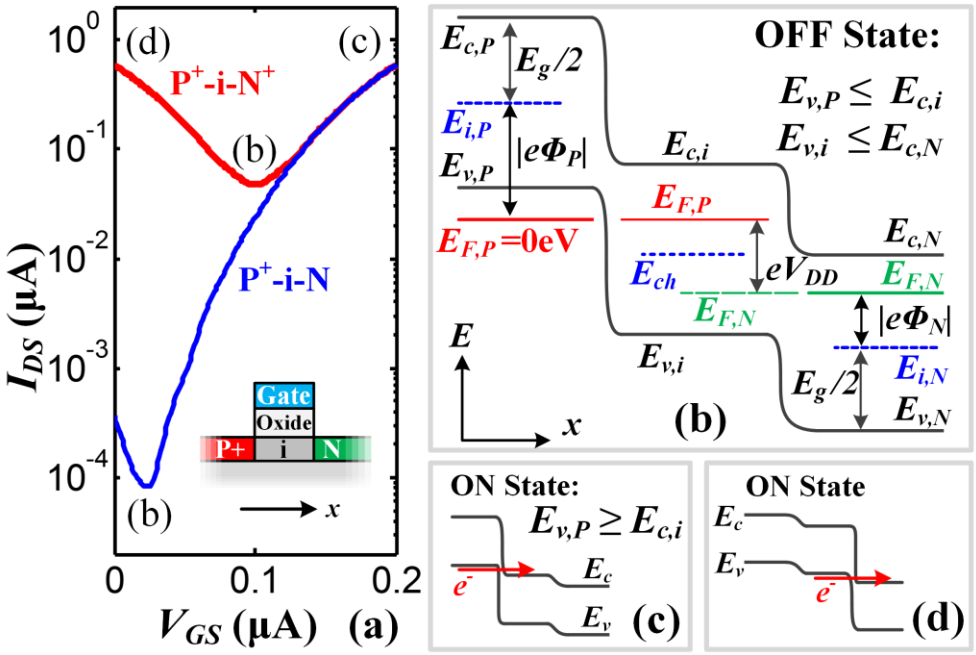


Figure 63: Design of GNR-TFETs for "all-graphene" circuits.

(a) V_{GS}-I_{DS} curves of P⁺-i-N⁺ and P⁺-i-N GNR-TFETs; Inset figure in (a) shows the device structure; (b-d) Band diagrams of (b) OFF state; (c) ON state and (d) ON state with tunneling at drain-channel junction. The V_{GS}-I_{DS} points corresponding to (b-d) are marked in (a).

According to **Figure 63b**, the interaction between doping and supply voltage (V_{DD}) is derived based on the criteria that an ideal NTFET should be fully ON (when V_G equals V_{DD}) or fully OFF (when V_G is 0) under any V_{DS} (0 to V_{DD}). **Figure 63b** shows that in OFF state, $E_{v,P} \le E_{c,i}$, where E_c is the bottom of the conduction band; E_v is the top of the valence band; subscripts *i*, *P* and *N* are for intrinsic, p-type and n-type regions. Another ON state where

tunneling occurs between channel and drain (**Figure 63d**) should be prevented by reducing the doping of drain so that $E_{v,i} \leq E_{c,N}$. E_{ch} is defined as the channel potential, which is $E_{ch} = E_{i,i} \sim (-eV_G)$, where e = +1.6×10^{-19} C. Since E_{ch} = 0 eV in OFF state (V_G = 0 V), $E_{v,i} \leq E_{c,N}$ and $E_{v,P} \leq E_{c,i}$ can be expanded to:

$$E_{ch} - E_g / 2 \leq E_{F,N} - eV_{DD} - |e\phi_N| + E_g / 2 \quad (8)$$

$$E_{F,P} + |e\phi_P| - E_g / 2 \leq E_{ch} + E_g / 2 \quad (9)$$

respectively, where |eΦ_P| and |$e\Phi_N$| refer to the Fermi potentials. $E_{F,P}$ is chosen as the 0 eV level. In ON state, $E_{ch} = -eV_{DD}$ and $E_{v,P} \geq E_{c,i}$, so that

$$E_{F,P} + |e\phi_P| - E_g / 2 \geq eV_{ch} + E_g / 2 \quad (10)$$

From (8) to (10), the interaction between doping and V_{DD} is roughly:

$$E_g - |e\phi_P| \leq eV_{DD} \leq E_g - |e\phi_N| \quad (11)$$

For instance, for the asymmetrically doped GNR-TFET simulated in **Figure 63**, a rough range of 0.05 – 0.2 V for V_{DD} can be determined.

Limitation of V_{DD} and doping of an isolated TFET was discussed as Equation (11). However, in the "all-graphene" circuit, parameters become more constrained when the interfaces between devices and interconnects are considered. In a typical PTFET/NTFET stack, which is required for designing complementary digital gates, drain-interconnect- drain (D-i-D) structures become relevant (**Figure 64a**). The D-i-D region in **Figure 64a** contains two doped drain regions and a graphene interconnect region.

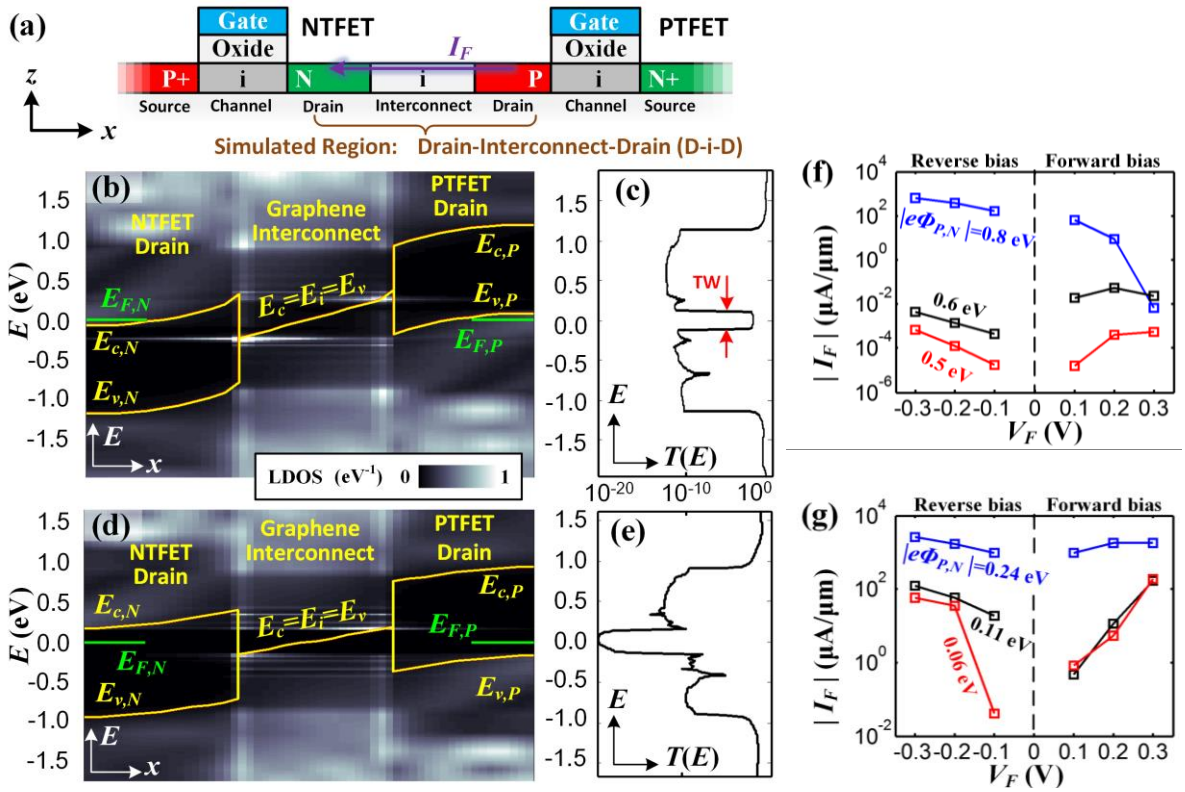


Figure 64. Simulation of drain-interconnect-drain regions.

(a) Schematic showing the simulated drain-interconnect-drain region; (b, d) Local density of states (LDOS) and band diagrams of the simulated region in (a) with (b) high doped drains ($|e\Phi_{P,N}|$ = 0.8 eV) and (d) low doped drains ($|e\Phi_{P,N}|$ = 0.5 eV). (c, e) Transmission spectrum ($T(E)$) of (b) and (d), respectively. TW is transmission window. (f, g) I-V curves of D-i-D regions: (f) N_W=6; (g) N_W=40. V_F and I_F denote the voltage and current from PTFET drain to NTFET drain, respectively. $|e\Phi_{P,N}|$ is the Fermi potential in the drain regions. Note that both $|e\Phi_{P,N}|$ and V_F affect TW.

To evaluate the properties of the D-i-D regions, a small D-i-D region is first simulated by real space NEGF with N_W=6 GNRs (W_{GNR} = 0.8 nm) and an infinite width graphene interconnect with 20 C atoms (2.1 nm) along length direction (with ac-chirality). Note that by TB approach, this chirality and dimension retain the band structure of graphene. The

Fermi potential of drains ($|e\Phi_{P,N}|$) is varied as 0.8, 0.6 and 0.5 eV.

Figure 64b,d show the band diagrams and local density of states (LDOS) of this region and **Figure 64c,f** show their transmission spectrum ($T(E)$). Its I-V characteristics are shown in **Figure 64f**. When drain regions are highly doped (**Figure 64b**, large $|e\Phi_{P,N}|$ = 0.8 eV), the current is high due to the tunneling window (TW) shown in **Figure 64c**. When drain regions have low doping, the current is limited and the TW vanishes (**Figure 64e**).

Hence, when designing all-graphene circuits, doping is limited by both Equation () (upper bound) and the transmission through the D-i-D structure (lower bound).

4. Benchmarking of Static Performance

An inverter chain based on the all-graphene design is shown in **Figure 62f**. According to the analysis and simulations above, the size parameters are optimized to: $W_{GNR} \leq 5$ nm, which allows a reasonable bandgap $E_g \geq 0.29$ eV; channel length L_{ch} = 22 nm, which is designed for comparison with CMOS; interconnect width and length are large enough ($X_{int} \times Y_{int} \geq$ 30nm×30nm) (**Figure 62f**) to ensure E_g =0 in graphene and low resistance **[57]**. TFETs are controlled by single gates with 1.2 nm oxide, where ε_{ox}=16. Doping are optimized as $|e\Phi_P|$ = 0.24 eV and $|e\Phi_N|$ = 0.12 eV for W_{GNR}= 5 nm, which satisfy the limitation from Equation (4) and provide considerable high current through the D-i-D region (I-V curves shown in **Figure 62g**).

Because the load inverter (Inverter 2) does not contribute to the static performances, the following discussion focuses on a single all-graphene inverter for simplicity. The working processes of an all-graphene inverter are described with band diagrams in **Figure 65**. Dashed lines are bands before charging/discharging (low-to-high/high-to-low transition) while solid lines are charged/discharged bands. When toggling, the output node (a D-i-D region including graphene interconnect and drain regions of both NTFET and PTFET), is

charged or discharged by band-to-band tunneling currents at source-channel interfaces. Subscripts *i*, *P* and *N* for E_c and E_v are omitted, and E_{FS} and E_{FD} represent Fermi levels for source for drain, respectively. When charging (or discharging), the bands of D-i-D region are shifted due to the changing of E_F of the output node ($-eV_{out}$).

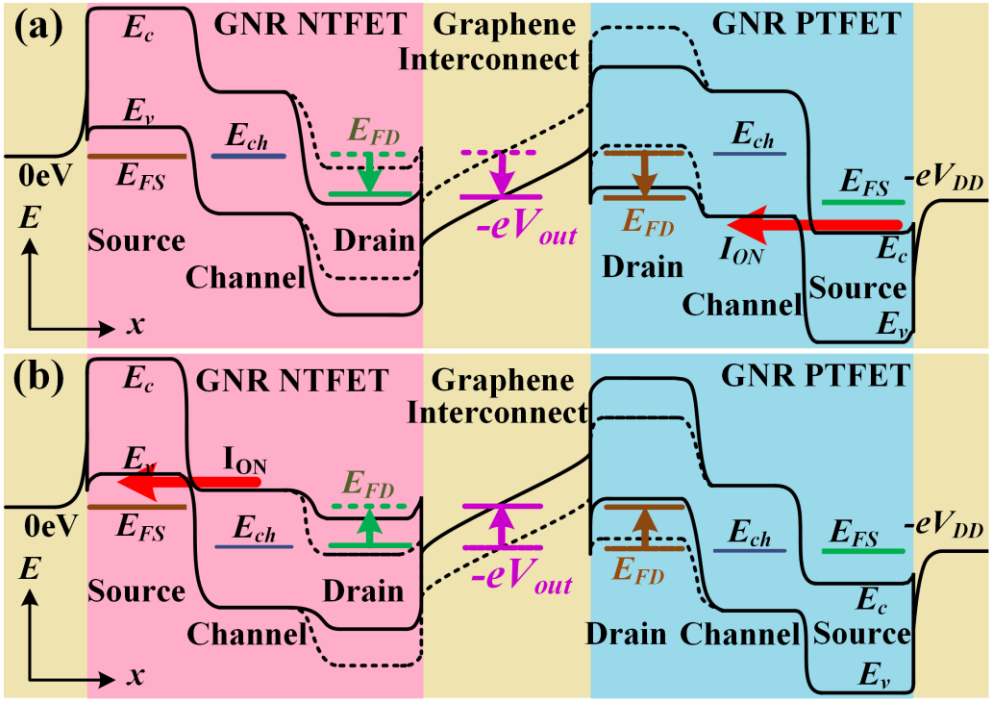


Figure 65. Band diagram of an "all-graphene" inverter.

Band diagram of an inverter showing (a) rising of output (V_{out} rises from low to high; dashed lines and solid lines represent bands before and after rising of output, respectively; and (b) falling of output (V_{out} falls from high to low; dashed lines represent bands before discharging and solid lines are discharged bands) of the output node (V_{out}); red arrows represent current directions.

Table 8: Normalized SNM (SNM/V_{DD}) and inverter gain vs. V_{DD}.

Note: When |Gain|<1, SNM does not exist according to the definition in Figure 66b.

V_{DD} (V)	22nm-CMOS		All-graphene	
	SNM /V_{DD}	|Gain|	SNM /V_{DD}	|Gain|
0.25	0.336	3.81	0.390	4.65
0.20	0.290	2.59	0.375	3.87
0.15	0.205	1.46	0.348	2.95
0.10	-	<1	0.290	1.99
0.05	-	<1	-	<1

Let channel size be $W_{GNR} \times L_{ch}$ = 5 nm × 22 nm. Source and drain lengths are set to 18 nm. Inverter voltage transfer curves (VTCs) for different V_{DD} are obtained by circuit level simulations based on lookup tables (I-V data for N- and P- TFETs, which are calculated by self-consistent NEGF-PE iteration loops). In **Figure 66a)**, solid lines represent all-graphene inverters and dashed lines represent 22 nm-CMOS LP model with minimum sizes. Inset plots are zoomed in around $V_{in} \sim$ 0.25 V. Normalized static noise margins (SNM/V_{DD}) and gain (defined in **Figure 66b**) vs. V_{DD} of CMOS and all-graphene inverters are listed in **Table 8**. Static noise margins (SNMs) shown are all low-noise-margins (=NM_L=V_{IL}-V_{OL}) while high-noise-margins (=NM_H =V_{OH} -V_{IH}) are no less than NM_L, where V_{IH}, V_{IL}, V_{OL} and V_{OH} are defined in **Figure 66b**.

When $V_{DD} \leq$ 0.2 V, output current I_{out} (the current flowing to output node) is always ~10^3 times the leakage (tunneling) current (I_{leak}) as shown in **Figure 67**. However, if V_{DD} > 0.2 V, when input is low (< 0.05 V), PTFET is ON but NTFET is incompletely OFF due to ambipolar behavior, which is an ON state as shown in **Figure 63d**. Hence, V_{out} is pulled down to 0.2475 V as shown in inset plot of **Figure 66a.** And the inverter suffers from an increased I_{leak}, which is nearly a decade higher than expected, resulting in a decade lower

I_{out}/ I_{leak} ratio, as shown in **Figure 67**. This effect reflects the upper bound for V_{DD} in Equation (4). On the other hand, a circuit level lower bound of V_{DD} appears around V_{DD} ~0.05 V where the SNM and |Gain| are unacceptably low (**Table 8**).

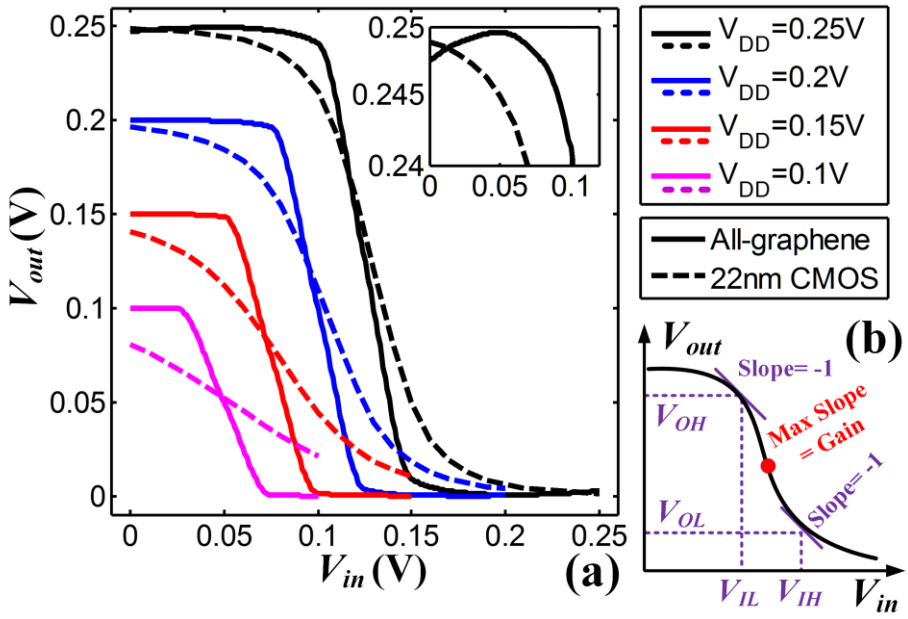


Figure 66. "All-graphene" inverter VTCs.

(a) Inverter VTCs for all-graphene circuits and 22 nm CMOS under different V_{DD}. Inset plot is zoom of (a) at V_{in} ~0.25 V. (b) definitions of gain, V_{IH}, V_{IL}, V_{OL} and V_{OH} for inverters.

The static power consumption for the all-graphene inverter is shown for different values of W_{GNR}, and compared to the 22 nm CMOS inverters. It can be observed that, the static leakage power P_{stat} of all-graphene inverter (W_{GNR} =5nm) is similar to that of 22 nm-CMOS HP model (**Figure 68**) with default threshold voltages. However, by decreasing W_{GNR}, E_g is increased, and I_{leak} is reduced significantly resulting in much lower P_{stat} than CMOS.

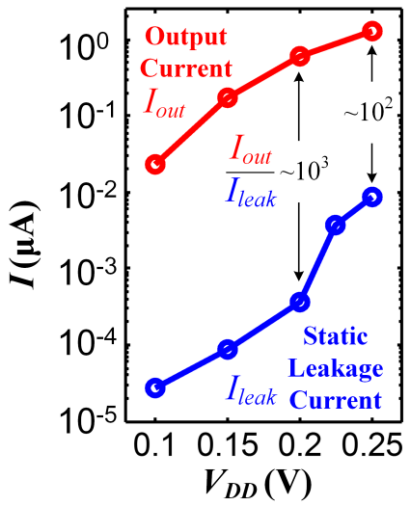


Figure 67. Static leakage current.

Plot of output current I_{out} (the current flowing to output node) vs. V_{DD} and static leakage current I_{leak} vs. V_{DD}.

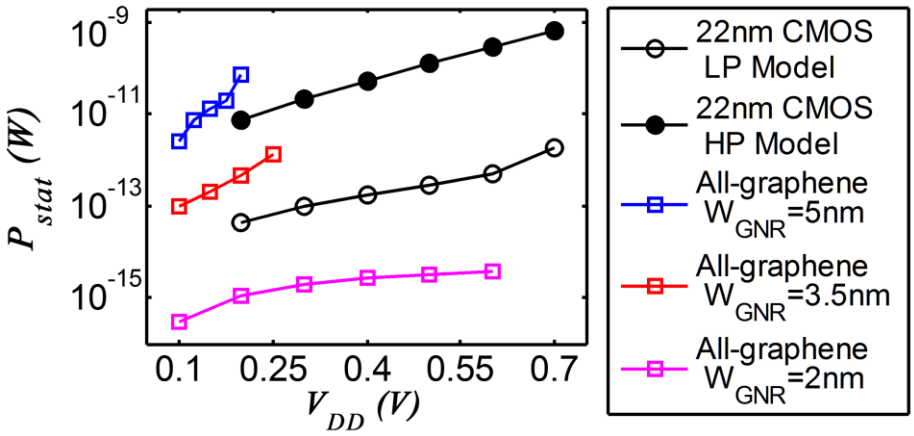


Figure 68. Comparison of static leakage power.

Static leakage power for 22 nm all-graphene inverters with different widths, in comparison with 22 nm CMOS inverters with default threshold voltages, plotted as a function of V_{DD}.

5. Benchmarking of Dynamic Performance

For evaluating the dynamic performance, it is necessary to estimate the load capacitances of an inverter in an inverter chain (Inverter 1 in **Figure 62**). The load capacitances in the inverter chain are shown in **Figure 69**, and include the following three components:

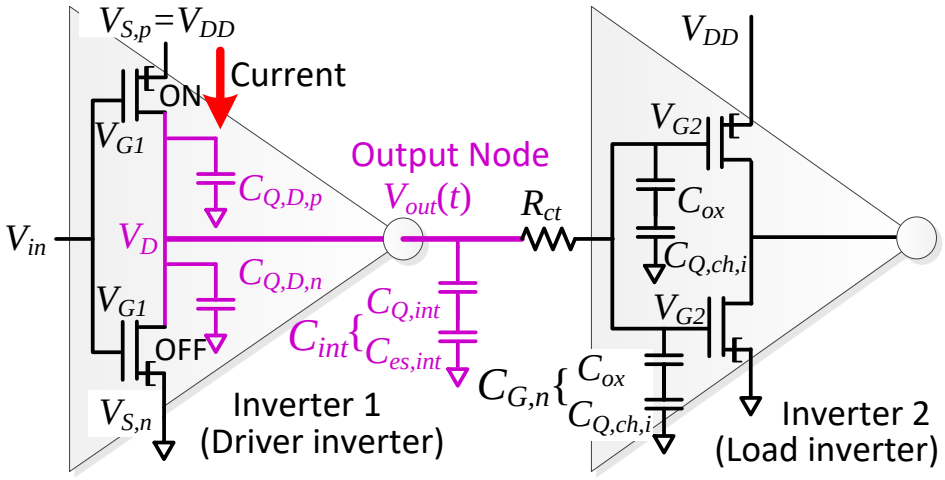


Figure 69: Capacitances in the inverter chain.

Load parasitics in and between driver and load inverters are shown.

i) Quantum capacitance (C_Q) of NTFET and PTFET drains in the driver inverter 1 ($C_{Q,D,p}$ and $C_{Q,D,n}$, respectively). $C_{Q,D,p}$ and $C_{Q,D,n}$ have the value of $C_{Q,D}$ = 0.7 pF/cm from NEGF by applying the method in **[279]** for W_{GNR} =5 nm.

ii) Graphene interconnect capacitance (C_{int}) (including quantum capacitance $C_{Q,int}$ and electrostatic capacitance $C_{es,int}$). For width = 30 nm; pitch = 30 nm; dielectric thickness = 30 nm; dielectric constant = 2.5, capacitance per-unit-length, $C_{es,int}$, is 0.47pF/cm **[57]**. $C_{Q,int}$ is calculated by NEGF but $C_{es,int}$ dominates C_{int}. Total C_{int} (with width = 30 nm) is 0.42 pF/cm.

iii) Load inverter capacitance (including two gate capacitances (C_G=C_{ox}//$C_{Q,ch,i}$), where

C_{ox} is the gate oxide capacitance and $C_{Q,ch,i}$ is C_Q of intrinsic channels). C_{ox} is calculated by the compact model in **[279]**. $C_{Q,ch,i}$ is a function of V_G. As shown in **Figure 70c**, C_Q along x direction in the NTFET (in inverter 2 in **Figure 62**) is varied by gate voltage (V_G). x is the transport direction as shown in **Figure 62**. Due to the position of E_c and E_v being varied by V_G, $C_{Q,ch,i}$ and $C_G = C_{ox}//C_{Q,ch,i}$ are high when quasi-Fermi level (red dashed line in **Figure 70 a, b**) is above E_c due to high V_G. Hence, $C_{Q,ch,i}$ and C_G are affected by V_G as shown in **Figure 70d**. $C_{Q,ch,i}$ is not monotonically increasing because local density of states (LDOS) has ripples in conduction bands as shown in **Figure 70a,b**. Similar flat portions of C_G *vs.* V_G in **Figure 70d** can also be seen in **[279]**.

C_Qs are calculated using NEGF simulator by the method in **[279], [280]** and the quasi-Fermi level is calculated by the method in **[281]**. Parasitic resistances and capacitances at graphene-GNR interfaces are negligible if the circuit is sized according to **Section III.G.4**.

The contact resistance R_{ct} between graphene interconnect and metal (in **Figure 69** and **Figure 62**) is taken into account by scaling the measurement data in **[214]** by area. For a $0.01\mu m^2$ interconnect with Pd contact, the relative R_{ct} is calculated to be 37 kΩ.

Now considering these load capacitances and contact resistances, a time domain simulation for the inverter chain is accomplished by a time-dependent NEGF system as shown in **Figure 71a**. There are four NEGF modules (green blocks) including real space and mode space. Each NEGF module consists of an NEGF-PE self-convergent iteration loop as shown in **Figure 71b**, where NEGF calculates carrier densities (ρ) from the potentials (U) given by 3D PE and then the PE calculates potentials using densities from NEGF. Real space NEGFs (2D NEGF formalism with 3D PE) are used to calculate transport in interconnects (heterostructure) modeled in 2D, while mode space NEGFs (1D NEGF formalism with 3D PE) are used to calculate transport in GNR TFETs, which can be

modeled as 1D transport.

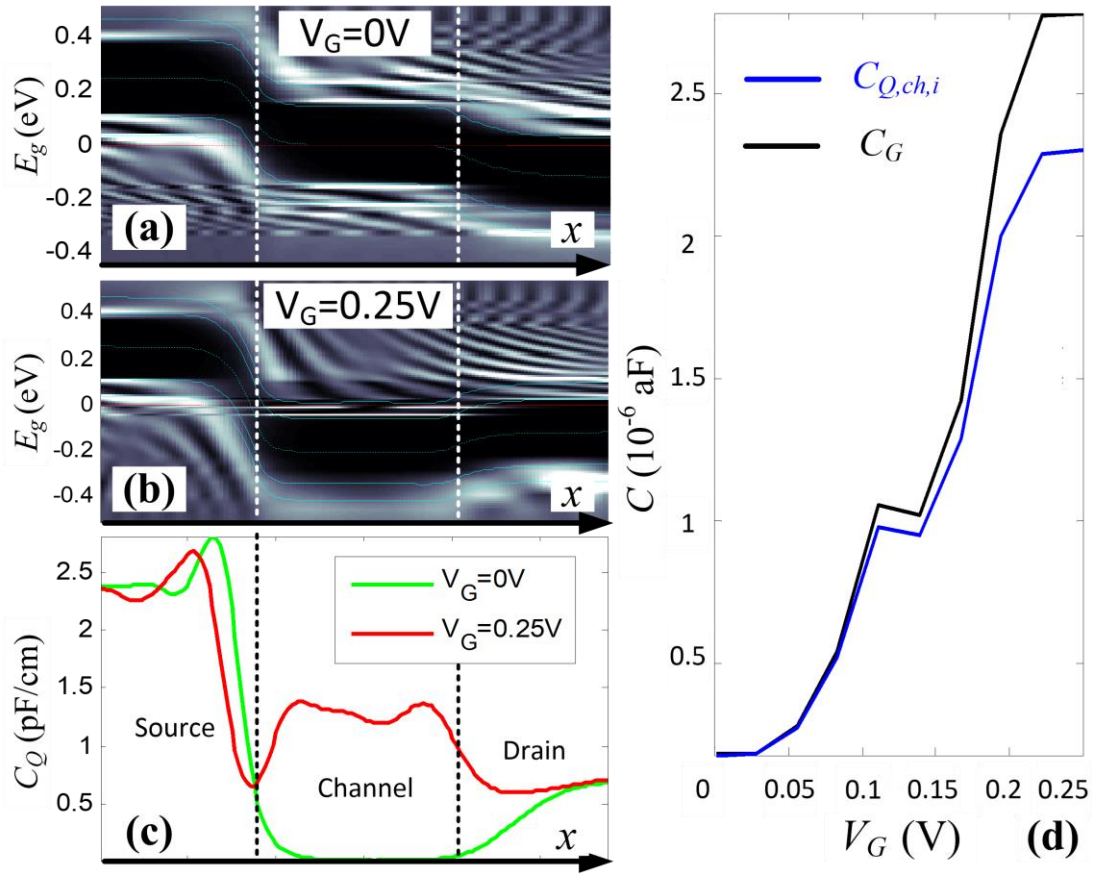


Figure 70: Quantum capacitance and gate capacitance.

(a) Local density of states (LDOS) in OFF state (low V_G); (b) LDOS in ON state (high V_G); Light blue lines in (a) and (b) are the first and second subbands; red horizontal lines represent E_F. (c) C_Q vs. x of the NTFET of inverter 2 in Figure 62 in ON state (V_G=0.25V) and OFF state (V_G=0V); (d) C_G and $C_{Q,ch,i}$ vs. V_G of P$^+$-i-N TFET when V_{DS}=0.

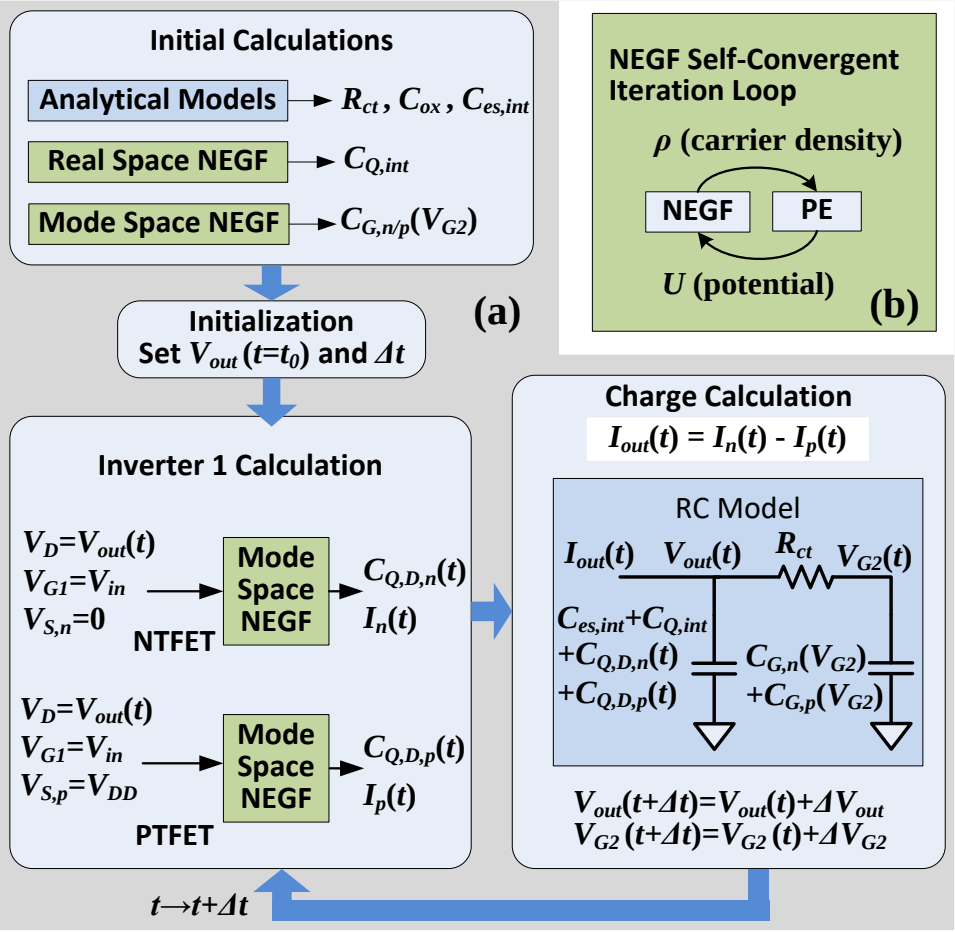


Figure 71: Time-domain NEGF-based circuit simulator.

(a) Schematic of the devised time-domain NEGF-based circuit simulator for inverter chain. (b) Schematic of the four NEGF modules (shown in green) in (a).

In the *Initial Calculations*, R_{ct} and parts of load capacitances (including C_{ox}, C_{int} and $C_{G,n/p}(V_{G2})$) are solved, where V_{G2} is the gate voltage in inverter 2 in **Figure 69**. Then in *Initialization*, the step length of the transient simulation, Δt and the initial value of V_{out} at $t=t_0$ is set. In *Inverter 1 Calculation*, transport is solved by NEGF with the input voltages $V_{S(n/p)}$, V_{G1}, and V_D (in **Figure 69**) determined by V_{DD}, GND, input voltage V_{in} and $V_{out}(t)$. After C_Q of drain regions ($C_{Q,D,n/p}$ (t)) and output current $I_{out}(t)$ are calculated, during *Charge Calculation*, charge flow in the circuit during $[t, t+\Delta t)$ are solved, using the RC model

shown in **Figure 71a**. Thereby, ΔV_{out} and ΔV_{G2} (the changes of V_{out} and V_{G2} respectively) are solved. Hence, $V_{out}(t+\Delta t)$ and $V_{G2}(t+\Delta t)$ can be solved. Next, t is set to $t+\Delta t$, and *Inverter 1 Calculation* and *Charge Calculation* are carried out with the new V_{out} and V_{G2} values, until $V_{out}(t)$ reaches a steady state.

Dynamic properties of the inverter chain with 0.01μm^2 of internal interconnect are evaluated. As shown in **Figure 71a**, 22 nm-CMOS models perform badly when V_{DD} is below 0.4V while all-graphene circuits work at V_{DD} ~ 0.1 V- 0.2 V with very low delays. In **Figure 71 b**, the dynamic power (P_{dyn}) vs maximum frequency (calculated from minimum delay) are plotted for both 22 nm-CMOS and all-graphene circuit and it is shown that all-graphene circuit consumes about 1-2 decades lower P_{dyn}) compared with 22 nm-CMOS at the same frequency. Hence, the proposed all-graphene logic design is also superior in terms of dynamic properties compared with those of 22 nm-CMOS, which is mainly due to the lower parasitic capacitances and the lower V_{DD} of all-graphene circuit.

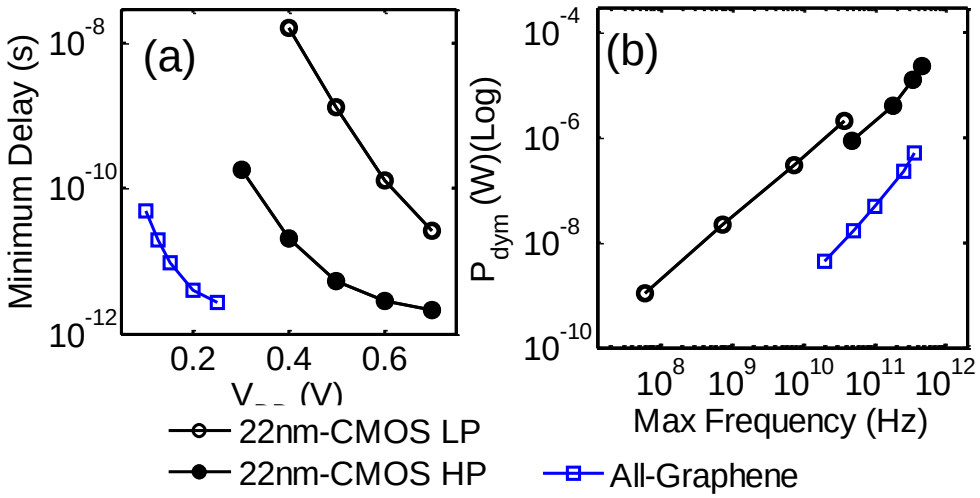


Figure 72: Dynamic properties of all-graphene inverter chain.

(a) time delay vs. V_{DD}; (b) P_{dyn} vs maximum frequency.

Note that the simulation scheme in **Figure 71a** is also suitable for simulation of large scale logic gates by increasing the numbers of NEGF modules and RC models, where each TFET corresponds to one NEGF module.

6. Summary of All-Graphene Monolithic Logic Circuits

In conclusion, band gap tuning induced by lithographic sketching of narrow/wide patterns on a single 2D monolayer graphene is proposed for exploring "all-graphene" ultra energy-efficient logic circuits based on GNR-TFETs. The proposed scheme is unique to graphene since it can be employed to fabricate both active and passive devices from the "same material" in a seamless manner. It is shown that the "all-graphene" circuit design scheme exhibits superior static performances with up to 1.7X higher SNMs, 1-2 decades lower static power consumption and 1-2 decades higher speed than that of LP as well as HP 22 nm-CMOS technology. Limitations on V_{DD} scaling are estimated theoretically and due to the smaller E_g of GNR, the minimum achievable V_{DD} is shown to be lower (0.1-0.2 V) than that of 22 nm-CMOS, which performs poorly when V_{DD} decreases to ~0.4V. Combined with the superior thermal, mechanical, and reliability properties of graphene, the "all-graphene" design scheme is envisioned to provide an attractive pathway for future ultra-dense 2D-electronics.

H. Summary of Metal Contacts

1. Summary of Computational Studies

The first half of this chapter presented a systematic and rigorous study of the physical nature of metal-TMD interfaces. The electron injection efficiency of the interfaces is shown to be characterized by three key criteria—tunnel barrier, Schottky barrier, and orbital

overlap. In order to accurately capture each of those criteria, DFT simulations incorporating semiempirical vdW potential are employed for the first time for metal-1L-TMD interfaces, and optimized geometries, effective potential, band structures, PDOS, valence electron densities, and bond Mulliken populations of metal-1L-TMD contacts are calculated. We find that Ti and Mo are the best top-contact metals for monolayer and multilayer intrinsic MoS_2 and are n-type contact metals. Pd is the best p-type top-contact metal for monolayer intrinsic WSe_2 while W can achieve high-quality n-type top contacts with WSe_2 due to the strong orbital overlaps and vanishing of Schottky barriers. While none of the metals studied in this work indicate the capability of forming good p-type contacts to MoS_2, from the basic interface physics revealed in this study, materials with strong orbital overlaps with MoS_2 have the potential to lead to such contacts. Such properties can possibly be found in molybdenum oxide compounds (MoO_x).

It is also shown that edge-contacted configurations can improve the contact by lowering tunnel barriers and strengthening the orbital overlaps. With the right metal and certain contact area, in order to achieve the lowest contact resistance, it is desirable to combine edge contact with top contact for monolayer TMDs. It can be inferred that inducing of edge contacts can be more significant for multilayer 1L-TMDs. For more-than-ten-layer TMDs, it is necessary to ensure that all of the edges are contacted to the metal using the tilt deposition technique **[282]**. On the other hand, it is possible to increase the edge contact length for lower contact resistance, for example, by cutting 1L-TMD edges into jagged edges. The results obtained in this study not only reveal the types of metals and configurations that can be employed for achieving low contact resistance with MoS_2 and WSe_2, but also highlight that the properties of contacts cannot be intuitively predicted by solely considering WF values (e.g., Au versus Pd; In versus Ti; Mo or W versus other metals).

Moreover, the significance of the developed framework, which features vdW interactions and bond Mulliken population analysis is apparent not only for contacts to various 2D materials, but also for understanding the nature of interfaces to a wide variety of 2D materials, which will be a key issue in optimizing the performance of all emerging 2D materials-based devices including the proposed concept of "all-2D devices and circuits" **[148]** (where graphene is used as gate electrodes and interconnects, MoS_2 and WSe_2 are used as channel materials in the FETs, and insulating h-BN is used as a gate dielectric). By combining our framework and transport simulations, quantitative values of contact resistances can be calculated in the future.

2. Experimental Review of Contact Resistances

Figure 73 gives the summary of contact resistances for 2D semiconductors found in the literature. From an experimental point of view, the contact resistance depends mainly on three parameters: contact metal, $\rho_{contact}^{2D}$ and the number of layers. This makes comparing contact resistance values found in the literature difficult because available data sets often differ by more than one parameter. Although results obtained using different metals are available, it is difficult to draw clear conclusions as to which metal yields the best contact to any given material from this meta-analysis. We nonetheless indicate for each study the contact metal. **Figure 73** shows the minimal R_C values from several studies on MoS_2 as a function of the number of layers **[5], [6], [42], [217], [218], [258], [283]–[287]**. Despite the scatter in the data, there is a clear trend of decreasing R_C with increasing thickness. This comes as no surprise, since the larger band gap in thinner flakes (red dashed line in **Figure 73**) is expected to give rise to larger Schottky barriers as well as the effects of edge contacts.

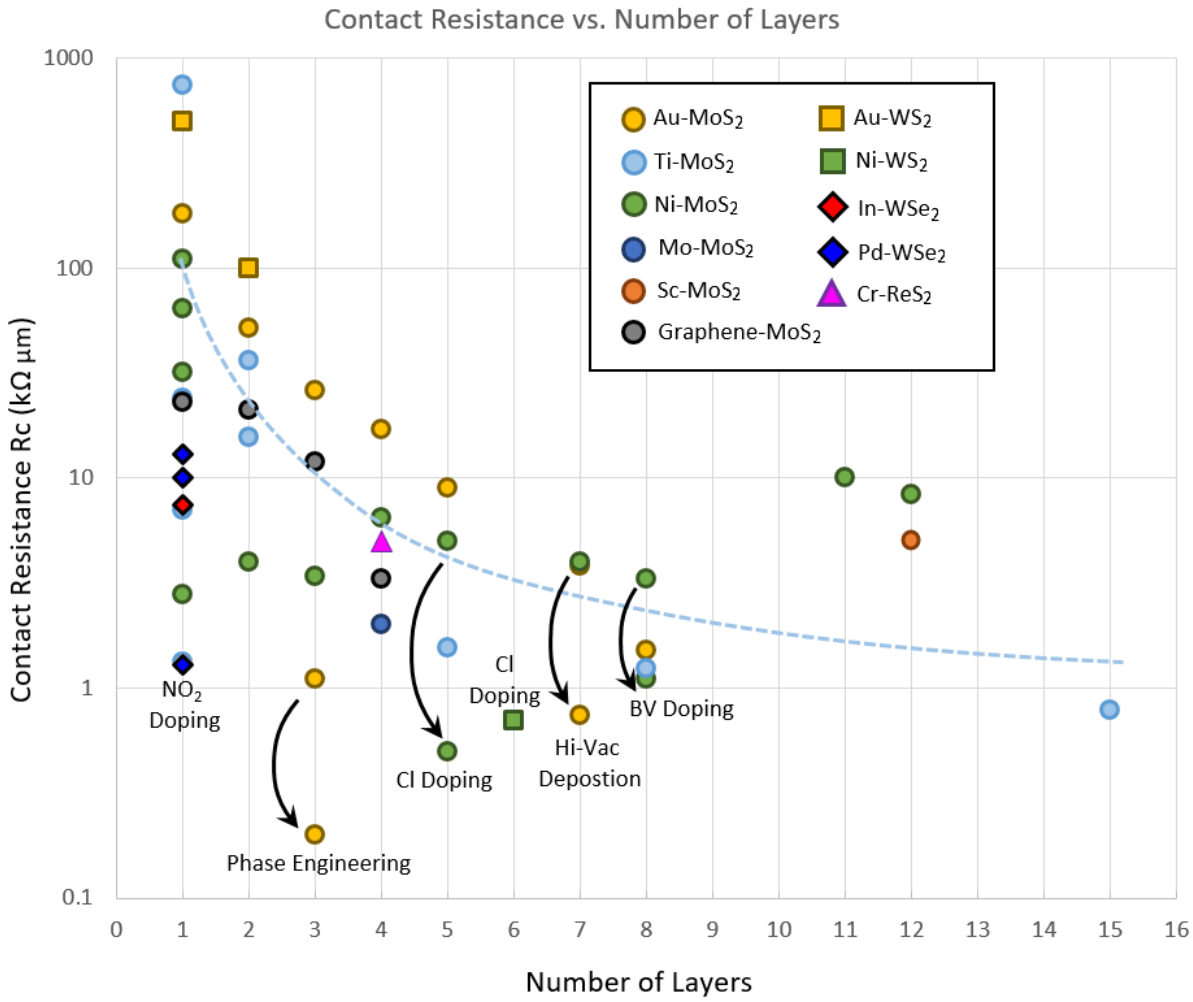


Figure 73. Contact resistance for 2D semiconductors.

Minimum contact resistance as a function of the number of atomic layers in several studies on MoS_2 as well as some other 2D semiconductors [5], [6], [42], [217], [218], [258], [283]–[287].

3. Chapter Summary

Realizing good electrical contacts is a prerequisite to harness the full potential of two-dimensional semiconductors. The atomic-scale thickness and pristine surfaces of 2D materials make it difficult to reduce the contact resistance. New theoretical models and

experimental approaches better suited to the low-dimensionality of the semiconducting material need to be developed. Recent years have shown impressive progress towards solving this problem. Several routes towards high-quality electrical contacts have been identified, the most promising of which is the realization of “seamless” electrical contacts, in which “native” chemical bonds allow much easier charge transport, and thereby lower contact resistances. For example, metallic TMDs can be used as covalently bonded electrical contacts to semiconducting TMDs, or sp^2 carbon-carbon covalent bonding is retained at the graphene-GNR junctions. However, most of the results so far were obtained on graphene and MoS_2. Material-specific properties such as the types of atoms and atomic defects can strongly influence the electrical properties. In this respect, our understanding of these contacts is still very limited and more systematic studies are needed, particularly in other TMDs.

IV. Other Interfaces of 2D Materials

A. Dielectric Interface and Mobility

Among various 2D materials, Molybdenum Disulphide (MoS_2) is considered as a promising candidate for next generation electronics. For applicability as electronic devices, a comprehensive understanding of the substrate/dielectric effects on MoS_2 is crucial, which is lacking at present. This chapter presents a systematic study of the interfaces between MoS_2 (monolayer and few layer) and its surroundings (substrates or dielectrics) using rigorous ab-initio density functional theory (DFT). Various surrounding materials are examined, including SiO_2, Al_2O_3, HfO_2, hexagonal BN (h-BN) and poly(methyl methacrylate) (PMMA). Key factors (dipoles and traps) affecting the mobility of MoS_2 are evaluated for various interfaces to MoS_2. Impact of different passivation treatments of the substrates is discussed as well.

1. Introduction: Impact of Substrates/Dielectrics

Compared to the conventional electronic materials such as silicon, 2D materials such as MoS_2, has pristine surfaces without dangling bonds, and ultra small thickness (6–7 Å/layer). These properties lead to few interface traps, excellent gate electrostatics, and reduction of short-channel effects and subthreshold leakage. Therefore, MoS_2 has been proposed as one of the promising candidates for next-generation transistors **[23]**, non-volatile memories **[288]**, and optoelectronic devices **[289]**.

However, the carrier mobility extracted from MoS_2 devices (i.e., 0.1-10 cm^2/Vs on SiO_2 substrate **[23]**) is much lower than the theoretical value (410 cm^2/Vs **[95]**). Such low mobility greatly limits the ON current as well as the switching speed of MoS_2 devices, and remains an essential issue. This phenomenon is caused by the interaction between the MoS_2

and its surrounding materials (substrates/dielectrics), which, unfortunately, is almost inevitable. Using a macroscopic view, it has been reported that high permittivity (high-*k*) dielectrics strengthen the confinement of electric flux and reduce Coulomb scattering **[94]** (mechanism 0 in **Figure 74a)**), which is believed to increase the carrier mobility in MoS_2 transistors **[23]**. However, a microscopic view of the physics of the MoS_2-substrate/dielectric interfaces as well as the effects of different substrate surface passivation treatments still remain unclear, especially the mechanisms shown in **Figure 74b**: 1a: surface dipoles (atomic groups), 1b: doping dipoles (formed by transferred charge), 2a: defect traps (localized states in substrate/dielectric) **[290]** and 2b: bonding traps (localized states at interfaces), all of which affect the mobility. These microscopic interface mechanisms play an important role in influencing the performance of MoS_2 devices, which is similar to those observed in other 2D materials such as graphene **[291]**. In this paper, using DFT, we comprehensively study the interfaces between MoS_2 and various surrounding materials and discuss the effects of different passivation treatments of the substrate surfaces. For surrounding materials, 3D bulk insulators (SiO_2, Al_2O_3 and HfO_2) are chosen to be studied due to their process robustness and electrical reliability. h-BN (2D) and PMMA (1D polymer fibers) are also evaluated because of their pristine surfaces. We show that apart from permittivity, the interface mechanisms are also critical for MoS_2 devices due to their influence on the mobility. Hence, to realize the maximum potential of MoS_2 devices by choosing a suitable surrounding material and its surface passivation treatment method, the interface mechanisms should be carefully evaluated using the simulation methodology introduced in this chapter.

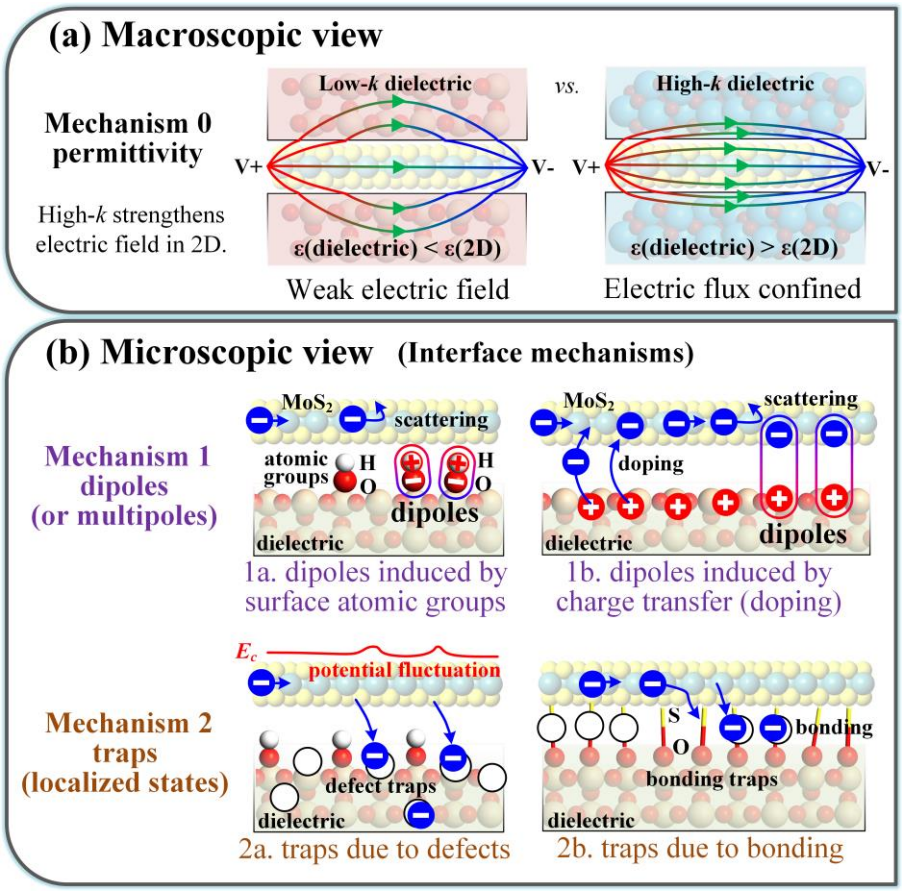


Figure 74: Mechanisms from surroundings that affect 2D material mobilities.

(a) Macroscopic view of mechanism (based on permittivity (ε)), where high-*k* dielectrics confine and strengthen electric flux in 2D channel materials, resulting in higher mobility.

(b) Microscopic view of mechanisms affecting mobility of 2D channel materials (interface mechanisms). Firstly, surrounding materials induce dipoles by surface atomic groups (1a: surface dipoles) and charge transfer (1b: doping dipoles). Secondly, traps are formed due to defects in surroundings (2a: defect traps) [290] or interface bonding between 2D channel and surrounding materials (2b: bonding traps). All these mechanisms can reduce mobility in 2D materials. E_c in (b) represents the conduction band of MoS_2.

2. Simulation Methodology for Understanding MoS_2 Interfaces

Since DFT only utilizes periodic boundary conditions, we chose interface unit cells that are periodical in *x* and *y* direction and separated by vacuum in *z* direction, as shown in **Figure 75a**. The unit cell contains a stack of intrinsic MoS_2 layer(s) and the surrounding material. For SiO_2, we chose a widely adopted crystalline phase (*I-42d* β-cristobalite) (**Figure 75b,c**), which is similar to amorphous SiO_2 in terms of local structure, density and refractive indexes **[292]**. While for Al_2O_3 and HfO_2, the corresponding crystalline phases are *r-3c* α-Al_2O_3 (**Figure 75d**) and *P21/c m*-HfO_2 (**Figure 75e**), respectively. To model a bulk oxide, the oxide thicknesses are chosen ≥ 10 Å (6-8 layers) and the dangling O atoms at the bottoms are terminated by hydrogen (H) and are fixed at bulk locations to reduce size effects **[293]**, while all other atoms are allowed to relax.

Numerical DFT calculations are performed using Atomistix ToolKit **[242]**. Local Density Approximation **[230]** are used for the exchange correlation potential due to its consistent accuracy for MoS_2 interface simulations **[1], [2]**. A double-ζ polarized basis set is used for expanding the electronic density. According to the dimensions of the unit cells, *k*-point samplings in the Brillouin zone are 4×8×1 for structures with SiO_2 or HfO_2, 4×4×1 for Al_2O_3 and 8×8×1 for PMMA or h-BN. Other parameters are density mesh cut-off =200 Ry and maximum force =0.05eV/Å for relaxation.

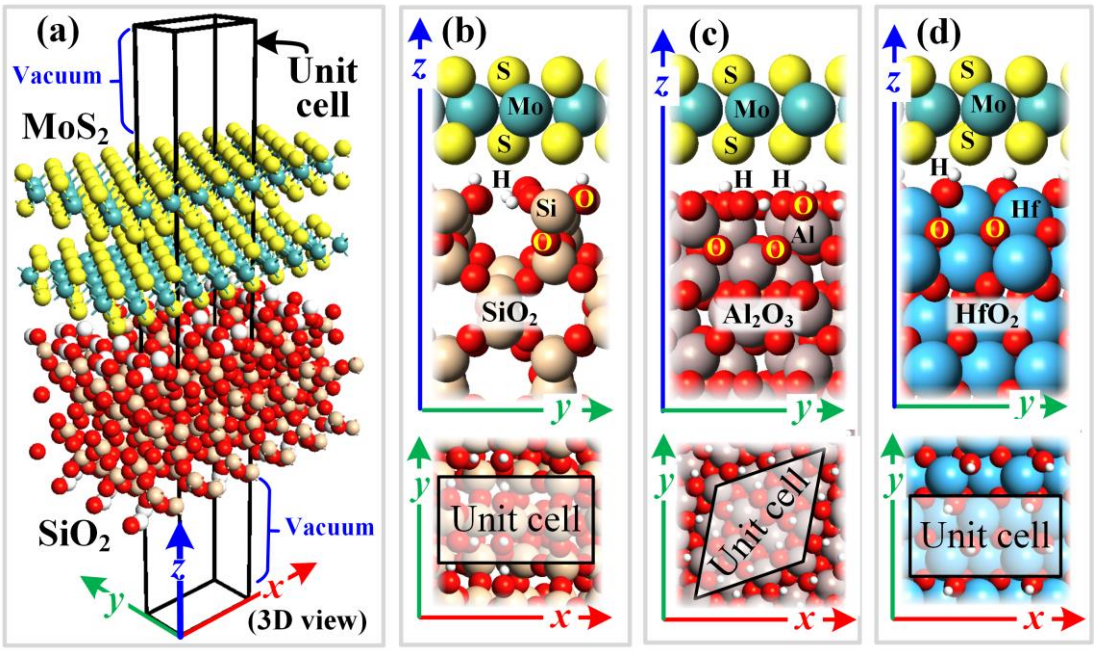


Figure 75: optimized geometry of 2D- bulk dielectric interfaces.

(a) 3D view of a relaxed unit cell (optimized geometry) consisting of a bilayer (2L) MoS_2 on SiO_2 with H-passivated surface, which is periodic in *x* and *y* directions. Vacuum regions above and below are used to separate periodic cells in *z*-direction. (b-d) *y*-*z* view (top) and *x*-*y* view in surrounding material layer (bottom) of relaxed unit cells with 1L MoS_2 on H-passivated (b) SiO_2, (c) Al_2O_3 and (d) HfO_2.

As shown in **Figure 76**, to study the interface mechanisms (traps and dipoles), four indicator terms are used, which are evaluated by DFT results (defined in **Figure 76** caption) – electron difference density (EDD), optimized geometry, partial density of states (PDOS), and band structure (*E*-*k*).

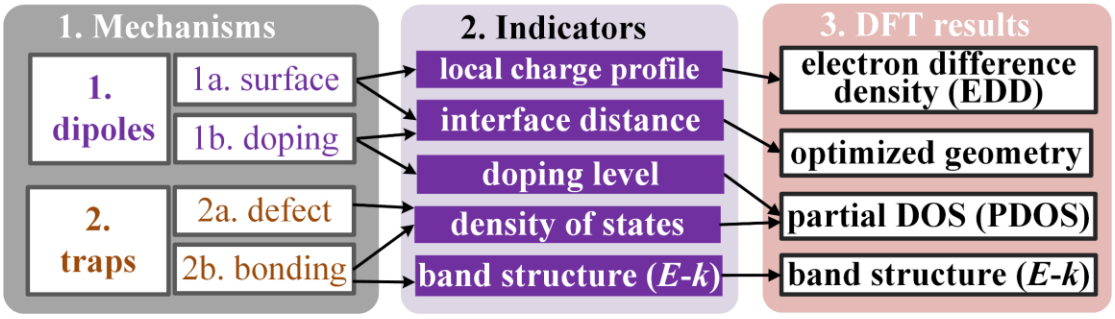


Figure 76: Evaluation of interface mechanisms by density function theory (DFT).

The three mechanisms in block 1 can be indicated by indicators in block 2. To evaluate the four indicators, DFT results in block 3 are used: Electron difference density (EDD) (difference between the actual observed electron density by DFT and superposed sphericalized atomic density), optimized geometry (relaxed configuration with minimum energy), partial density of states (Partial DOS, PDOS) (DOS on specified atoms and orbitals) and band structure (*E*-*k*).

3. H-Passivated Bulk Surrounding Materials

The optimized geometries, EDDs, and PDOS of interfaces between MoS_2 and H-passivated SiO_2, Al_2O_3 and HfO_2 are shown in **Figure 75**, **Figure 77**, and **Figure 78**, respectively.

Interface distance (Δz) and Fermi potential ($e\Phi_F$) are defined and listed in **Table 9**. In terms of surface dipoles (mechanism 1a), Al_2O_3 has the lowest influence on 1L MoS_2 due to the large dipole depth (**Figure 77b**), while 1L MoS_2 with HfO_2 suffers from shallow dipoles in HfO_2 (**Figure 77c**). Similarly, due to the largest Δz (**Figure 75c** and **Table 9**), Al_2O_3 has the lowest doping effect (**Figure 78c**), while HfO_2 induces much more doping (**Figure 78d**), indicating that doping dipoles (mechanism 1b) are the fewest from Al_2O_3 (Al_2O_3 < SiO_2 < HfO_2).

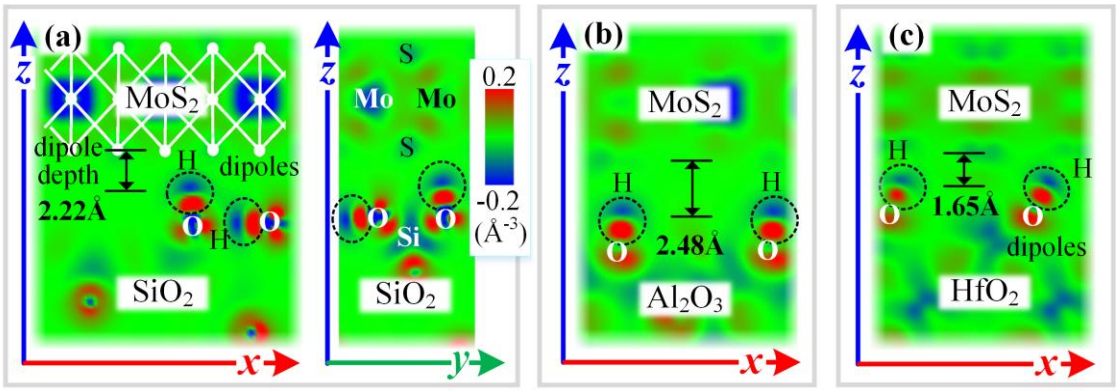


Figure 77: EDD contour of interfaces.

EDD contour of interfaces between 1L MoS_2 and H-passivated (a) SiO_2, (b) Al_2O_3 and (c) HfO_2. Color bar in (a) is shared by (a-c). OH atomic groups form dipoles (circled) in dielectrics. The dipole depth (~interface distance) is measured from the centers of S atoms to the centers of hydroxyl (OH) atomic groups. Color bar in (a) is common for all contours

PDOS of trap states are shown and compared in **Figure 79a**, where HfO_2 induces much more traps than SiO_2 and Al_2O_3. These localized states are created by the overlap of orbitals between MoS_2 and HfO_2 (mechanism 2b) as shown in **Figure 79b**, which have high effective mass and reduce the mobility. Hence, in terms of interface mechanisms, the influence on mobility can be sorted by Al_2O_3 < SiO_2 < HfO_2, the first two of which are confirmed by experiments (**Figure 80**).

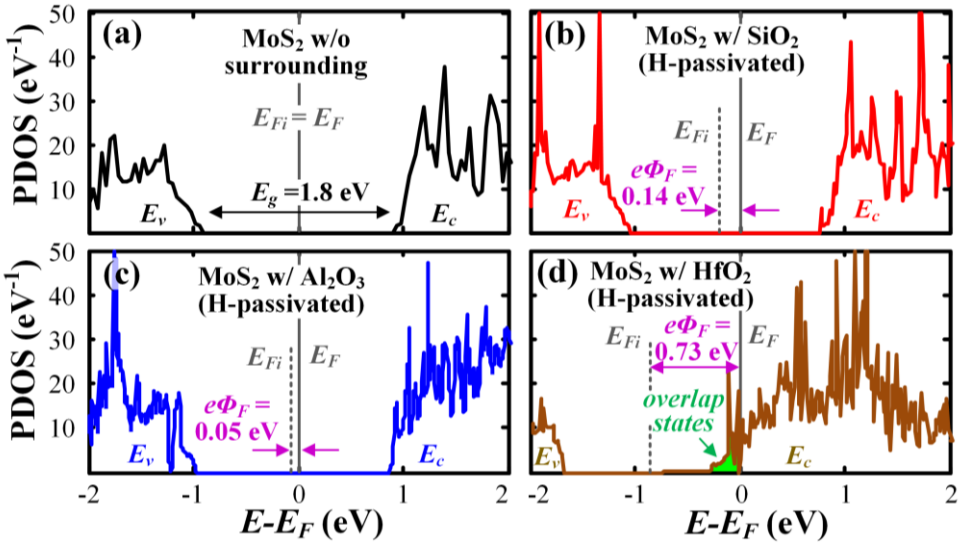


Figure 78: Partial DOS (PDOS) of 1L MoS_2.

(a) Without (w/o) any surrounding; (b-d) with (w/) passivated (b) SiO_2, (c) Al_2O_3 and (d) HfO_2. Doping effects (Fermi potential $e\Phi_F$) are sorted by Al_2O_3 < SiO_2< HfO_2, indicating MoS_2-Al_2O_3 interface forms the least numbers of dipoles. For (d) HfO_2, overlap states appear in the band gap, which may form traps.

For bilayer (2L) MoS_2, due to the increase of MoS_2 volume and Van der Waals force from the upper layer, the interface distances between bottom layer MoS_2 and substrates increase, thereby reducing the substrate doping effect according to DFT results (**Table 9**). Hence, the influences from surface dipoles (mechanism 1a) and traps (mechanism 2) are weakened compared with monolayer MoS_2. Also, doping dipoles (mechanism 1b) are much less, resulting in mobility increase (last column in **Table 9**).

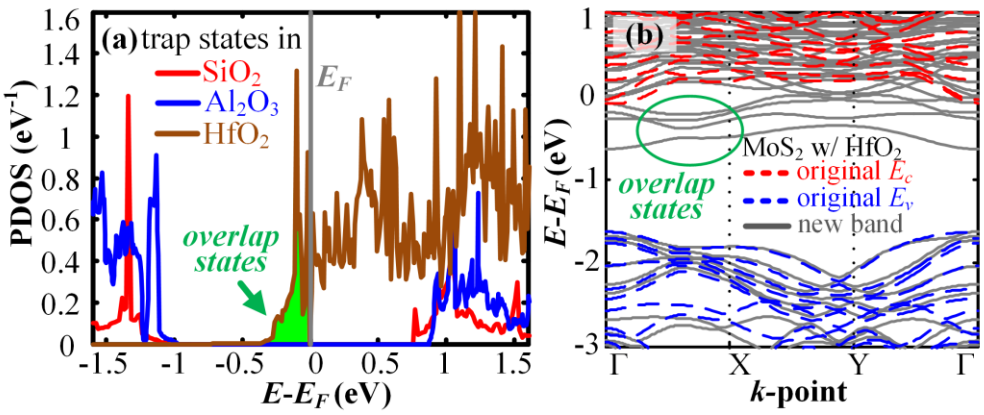


Figure 79: Trap states in bulk surrounding materials.

(a) PDOS of atoms in the first 3 layers in bulk surrounding materials showing the trap states; (b) band structure of original MoS_2 and distorted band structure of MoS_2 with passivated HfO_2. Overlap states form bands with high effective mass in band gap, which act as bonding traps that reduces mobility (mechanism 2b).

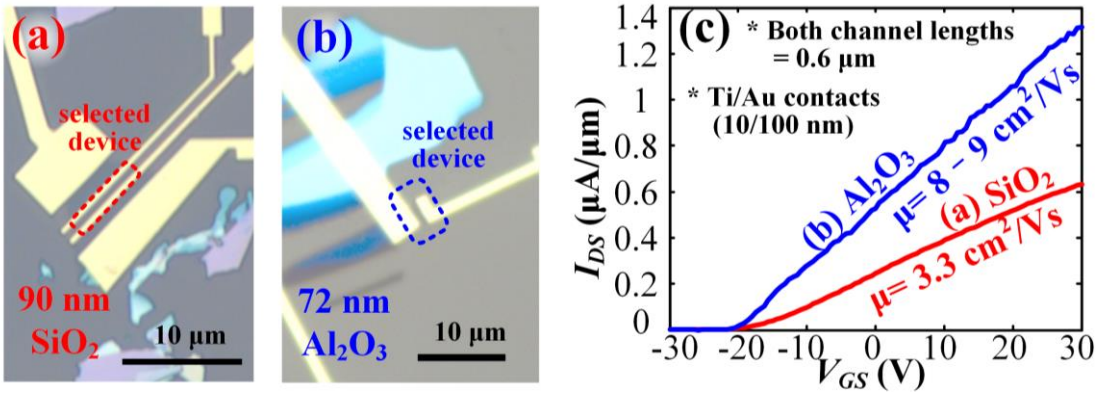


Figure 80: Influence on mobility confirmed by experiments.

Microscope photos for 1L MoS_2 FETs fabricated on (a) SiO_2 substrate and (b) Al_2O_3 substrate. (c) Transfer characteristics of (a) and (b) with normalized EOT. Due to the interface mechanisms, device on Al_2O_3 substrate gives higher measured mobility.

Table 9: Data for selected interfaces.

Permittivity ($\varepsilon/\varepsilon_0$) w.r.t that of vacuum, passivation method, interface distance (Δz, average distance between S atoms and the surface atoms in surrounding materials), Fermi potential ($e\Phi_F = E_F - E_{Fi}$) of each interface, doping density (on MoS_2 induced by surrounding materials, calculated by DFT) and experimentally measured mobility.

# of MoS_2 layers	surrounding material	$\varepsilon/\varepsilon_0$	passivation method *	Δz (Å) *	$e\Phi_F$ (eV) *	doping density (cm^{-2}) *	μ (cm^2/Vs)
1L	SiO_2	3.9	H	2.02	0.14	1.8×10^{0}	<4 **
2L				2.13	0		21 **
1L			CH_3	2.19	0.15	2.9×10^{0}	N/A
1L	Al_2O_3	8-9	H	2.52	0.05	5.5×10^{-2}	13 **
2L				2.60	0		>25 **
1L	HfO_2	16-25	H	1.87	0.73	2.1×10^{13}	15 #
1L	h-BN	~4		3.15	0		N/A
1L	PMMA	~2-4		2.00	0		N/A
* calculated by DFT; ** Back-gated devices measured under V_{DS} =0.1 V; # Top-gated devices from **[23]**.							

It is important to mention that these bulk surrounding materials suffer from defect traps (mechanism 2a) inside the bulk (**Figure 81a)**), resulting in the potential fluctuation (**Figure 81b**) and thus in reduction of mobility, which is also confirmed by **[290]**.

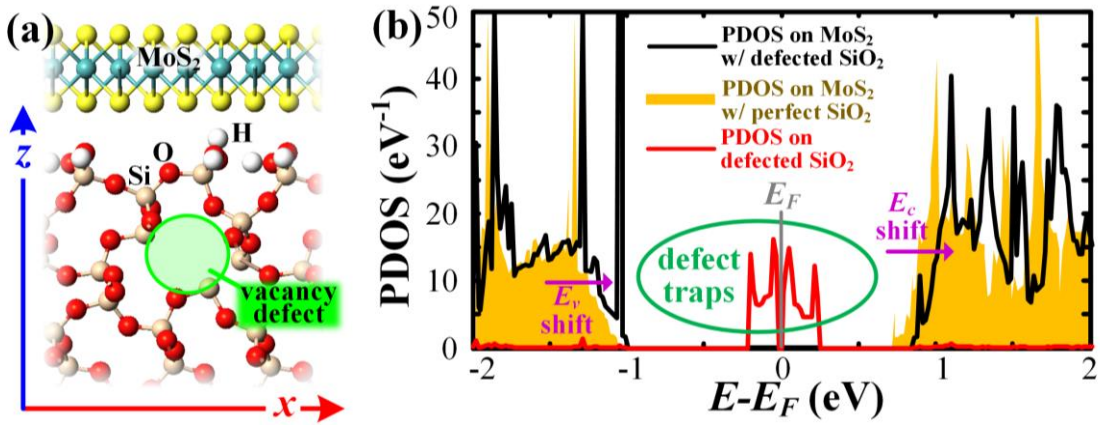


Figure 81: 1L MoS_2 on SiO_2 with a vacancy defect.

(a) Relaxed cell (optimized geometry). (b) PDOS of MoS_2 and SiO_2 in (a). MoS_2 electrons are trapped by the defect in SiO_2, resulting in shift of E_c/E_v to higher energy with respect to Fermi level. This effect can cause potential fluctuation in MoS_2 (mechanism 2a) and hence, reduce the mobility.

4. Passivation Treatments

Taking SiO_2 as an example, thermal grown SiO_2 surface is usually terminated by H (**Figure 75a,b**). However, in case of defected surfaces (O-terminated surfaces), interface bonds (S-O bonds) are formed between SiO_2 surface and MoS_2 (**Figure 82a,b**), which undermine the band structure of MoS_2 (**Figure 82c,d**), leading to the buildup of interface traps (mechanism 2b). Moreover, *E-k* distortion is observed in the original E_c/E_v, where bands are flattened (**Figure 82c**) resulting in the increase of carrier effective masses and thus, in reduction of mobility. In the worst case of *E-k* distortion, device failure may even happen.

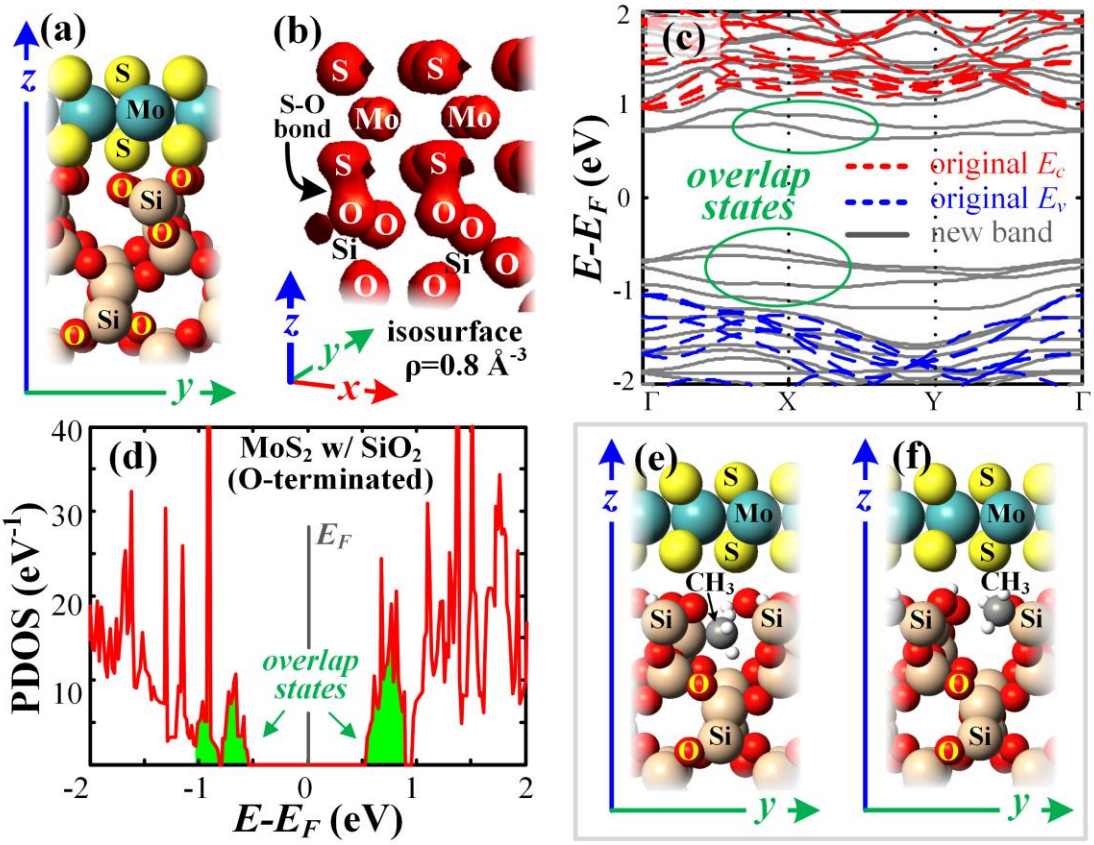


Figure 82: Effects of passivation treatments.

(a) relaxed unit cell of 1L MoS_2 on SiO_2 with unpassivated surface terminated by O.

(b) electron density isosurface of (a). Isosurface value is 0.8 $Å^{-3}$. S and O atoms are found to be covered by the isosurface indicating formation of S-O bonds.

(c) band structure of (a), compared to original MoS_2. Overlap states form bands with high effective mass in band gap, which act as traps that reduce mobility. Moreover, some of the original bands are flattened, resulting in higher effective mass and lower mobility.

(d) PDOS of MoS_2 in (a). Overlap states (bonding traps) appear in the band gap. (e, f) relaxed unit cells of 1L MoS_2 on passivated SiO_2 terminated by H and CH_3 groups.

(e) and (f) are two samples with CH_3 at different positions. As shown in Table I, these two samples form similar doping density with the H-terminated sample but slightly larger interface distances, indicating that the introduction of CH_3 groups on SiO_2 surface by HF dipping can weaken the scattering from traps and dipoles to some degree, which is similar to the case of graphene devices [291].

HF-dipping treatment induces methyl (CH_3) atomic groups at SiO_2 surface, hence reducing the charge transfer by enlarging Δz, which increases the carrier mobility in graphene devices **[291]**. For the case of MoS_2, the same treatment is evaluated using the interfaces shown in **Figure 82e,f**. Though the results show a similar doping level in MoS_2 with H-terminated SiO_2, however, an increased Δz is found. Hence, HF-dipping treatment can slightly reduce the formation of doping dipoles (mechanisms 1a) and weaken the scattering from dipoles and traps in SiO_2 (mechanisms 1b, 2a).

5. Low-Dimensional Dielectrics

Interfaces between 1L MoS_2 and h-BN (**Figure 83a**) or PMMA (**Figure 83b-d**) are evaluated. Interface with h-BN shows the largest depth from MoS_2 to dipole (or multipole) centers (**Figure 83e**), while PMMA induces shallow dipoles (multipoles) near the interfaces (**Figure 83f**), which affect the mobility in MoS_2 (mechanism 1a). However, both materials do not show any charge transferred to MoS_2 (**Figure 83g**). Thus, they are free from doping dipoles (mechanism 1b). Moreover, due to less crystal defects (mechanism 2a) and less dangling bonds (mechanism 2b) in low-dimensional materials, the amount of traps is much less compared with bulk materials.

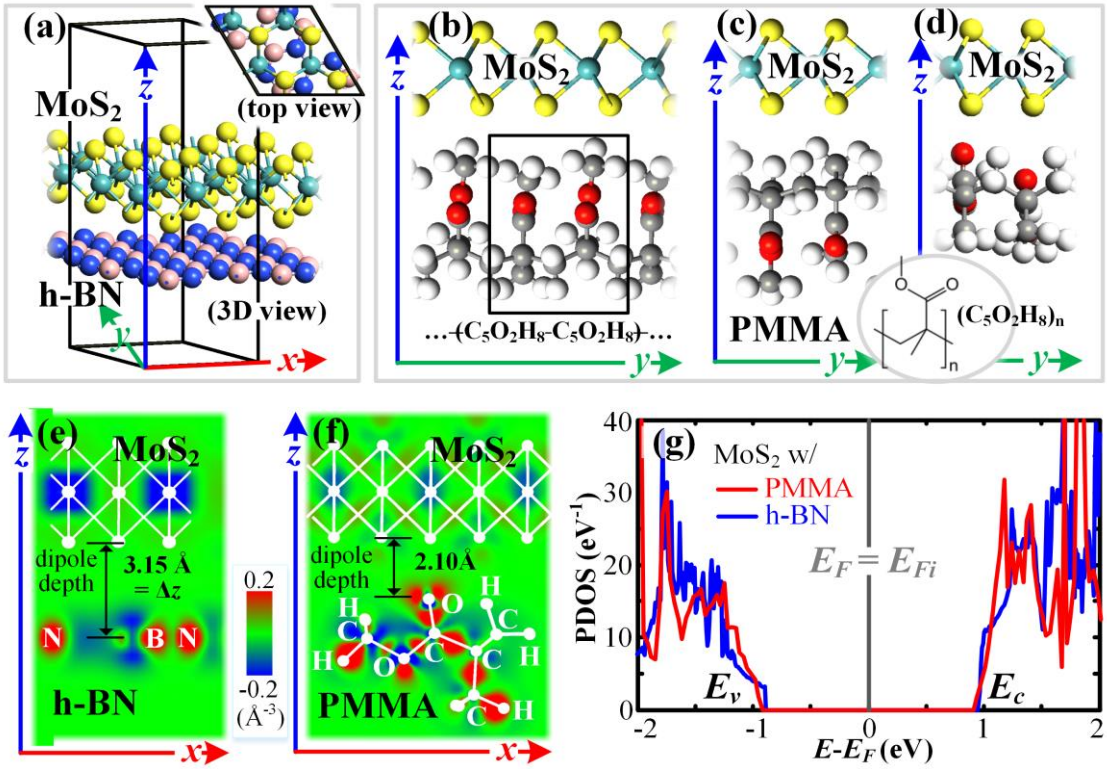


Figure 83: Interface with low-dimensional surroundings.

(a) 3D view of the relaxed unit cell consisting of interface between 1L MoS_2 and h-BN. Inset figure shows the top view (*x*-*y* view). (b-d) views of the relaxed unit cells with 1L MoS_2 and PMMA. (b-d) are 3 samples with different PMMA orientations. Inset figure shows the repeating unit and molecular formula of PMMA. (e) EDD of (a). (f) EDD of (d). Interface with h-BN has the largest dipole (multipole) depth while interface with PMMA has very shallow dipoles (multipoles), indicating that the strength of dipole scattering from h-BN is weakest while PMMA may induce strong scattering in MoS_2 thereby degrading its mobility. (g) PDOS of MoS_2 with h-BN and PMMA. Since MoS_2 in sample (b-d) show similar PDOS, only PDOS of MoS_2 in (d) is shown. Both surrounding materials do not dope MoS_2.

6. Summary of Section

Using DFT, interfaces between MoS_2 and various substrates /dielectrics are studied in this work. According to **Figure 84**, Al_2O_3 is recommended as substrate /dielectric for MoS_2 due to its greatest potential to preserve the carrier mobility in MoS_2. Moreover, for devices with SiO_2 or Al_2O_3, few layer MoS_2 is recommended due to weakening of interface mechanisms and increase of mobility. Dipoles and traps in HfO_2 may offset its benefits arising from high permittivity. Moreover, a proper passivation treatment of bulk substrates is a necessity. Both h-BN and PMMA does not dope MoS_2, but PMMA induces surface dipoles that reduce MoS_2 mobility. h-BN is advantageous in terms of interfaces, but its permittivity limits its use for boosting the mobility. It is recommended to use h-BN as a buffer layer between high-*k* materials and MoS_2 in order to take advantage of both surrounding materials. This is similar to the low-*k* polymer buffer layer added between high-*k* dielectric and graphene to minimize the scatterings **[294], [295]**

This study not only revealed the types of surrounding materials that can be employed in device/process design for achieving high performance, but also highlighted that apart from permittivity, the interface mechanisms are critical for MoS_2 devices due to their influences on the mobility. Moreover, the significance of the simulation methodology is apparent for a broad range of 2D materials.

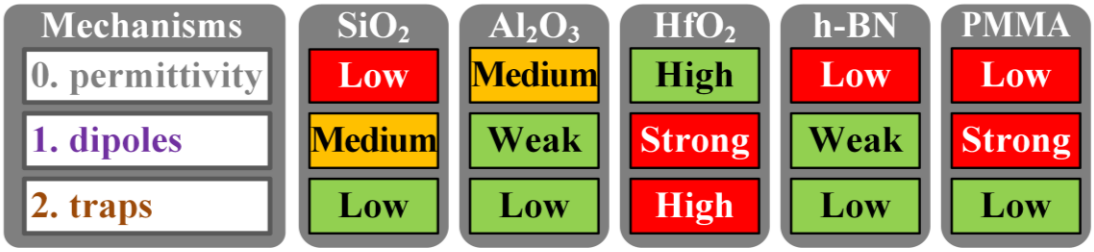


Figure 84: Summary of the surrounding mechanisms that affect mobilities.

Overall, Al_2O_3 shows the greatest potential to preserve the intrinsic mobility in MoS_2. Interface mechanisms (1,2) in HfO_2 may offset its benefit from permittivity (mechanism 0). Hence, the mobility increase by using HfO_2 is quite limited (Table I). In terms of interface mechanisms, h-BN is the best surrounding material, which is also confirmed in graphene devices [154]. However, since its permittivity is lower than that of MoS_2 (ε(graphene)<ε(h-BN)<ε(MoS_2)), the mobility boost in MoS_2 devices may not be as effective as that in graphene devices, which can be explained by mechanism 0.

B. Substrate Effects during Growth

At the high substrate temperature during a typical process (~ 950 ºC), the passivation layer formed by the -OH groups on top surface of SiO_2 layer can be detached as H_2O molecule leaving an O-terminated SiO_2 surface. Such surface, during MoS_2 growth, can react with S, oxi-sulfide of Mo, as well as the grown MoS_2; while during WSe_2 growth, it can react with W, oxi-selenide of W, as well as the grown WSe_2.

1. Effects of Interface Bonding

DFT simulations capture the phenomenon that chemical bonds such as O-S / O-Se bonds are formed at the interface between MoS_2 / WSe_2 and the substrate, as illustrated in **Figure 85b,e** and **Figure 86a**. These bonds not only act as interfacial charge traps, which are localized, but also induce band structure distortion (**Figure 85h,i** and **Figure 87a**). Both

effects can degrade the mobility.

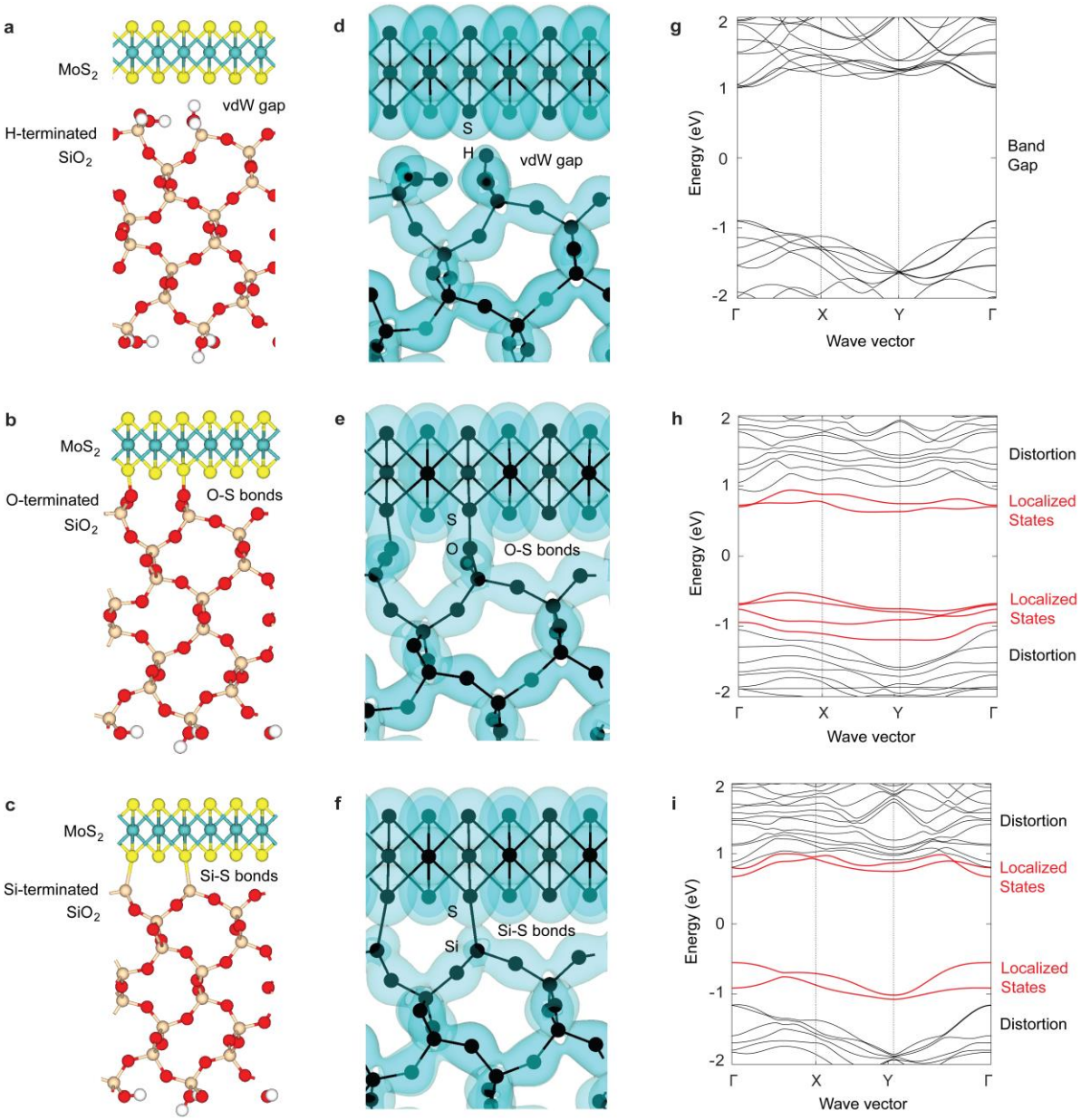


Figure 85: DFT results illustrating the substrate temperature effect for MoS_2.

The bond Mulliken populations of Si-O bond in SiO_2, interface H-S bond, interface O-S bond and interface Si-S bond are compared in **Table 10**. It can be seen that the interaction between H atoms of the passivated SiO_2 surface and the S atoms of MoS_2 is purely vdW

type, which can preserve the pristine surface of MoS_2. While the interface O-S bonds due to high process temperature are strong covalent bonds, which disturb the band structure of MoS_2 with no doubt.

Table 10: Bond strengths and types in Figure 85.

	Bond Mulliken Population m	Bond type
Si-O bond in SiO_2	1.025	Covalent
Interface H-S bond	0.135	vdW
Interface O-S bond	0.846	Covalent
Interface Si-S bond	0.409	Weak covalent

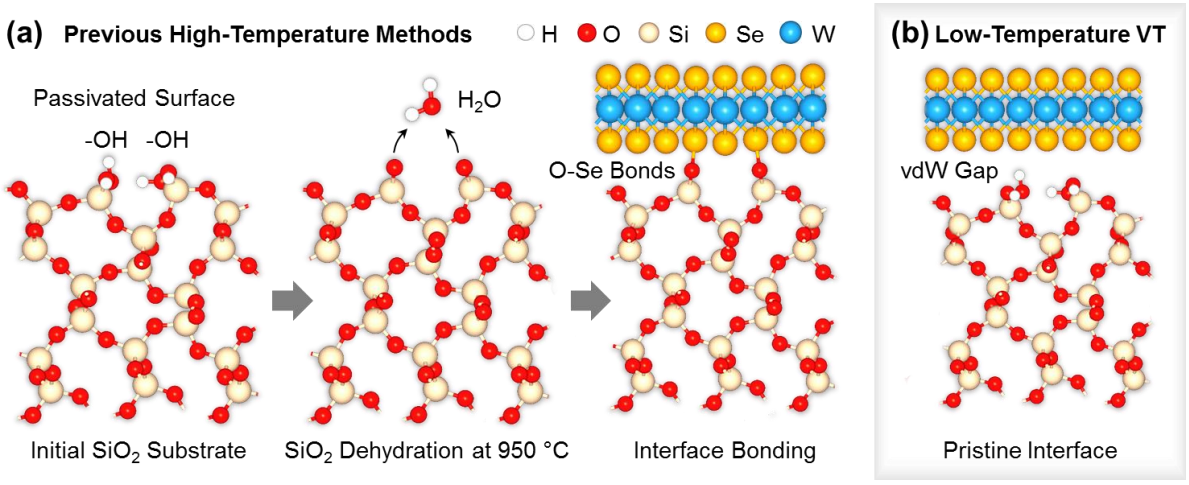


Figure 86: DFT results illustrating the substrate temperature effect for WSe_2.

(a) During a high-temperature process (~ 950 °C), SiO_2 substrate gets dehydrated leaving bare oxygen atoms on the surface, which form interfacial O-Se bonds with WSe_2. (b) The low-temperature vapor transport (VT) process (~ 650 °C) can minimize interface bonding and form van der Waals gap type interface, which retain the pristine properties of WSe_2.

2. Saturated Substrate Surface

Hence, a lower process temperature is preferred from the aspects of not only thermal budget but also crystal quality (**Figure 85a,d,g**). As shown in **Figure 86b**, use of relatively lower temperature (650 °C) in vapor transport method can reduce the possibility of interface traps, and thus preserve the pristine interface of WSe_2 (**Figure 87b**), inevitably benefiting the mobility and the device reliability.

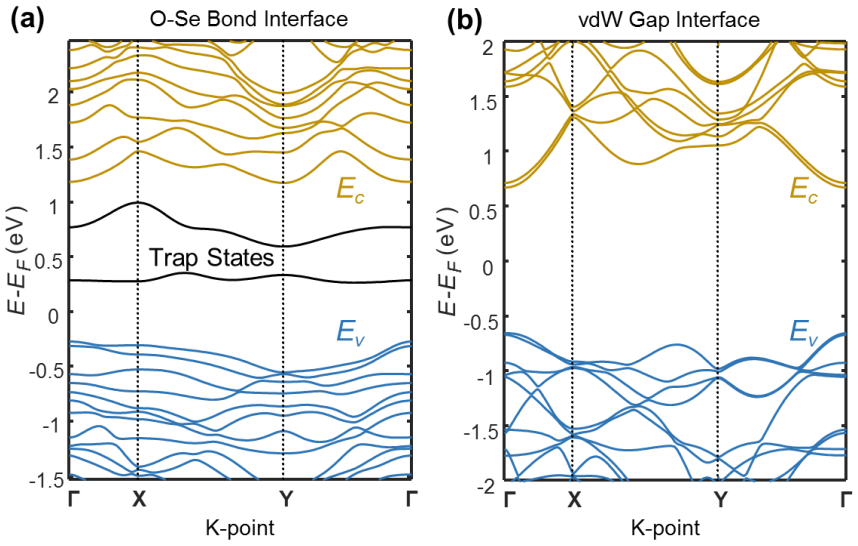


Figure 87: Effect of interface O-Se bonds on the band structure of WSe_2.

(a) WSe_2 suffering from interface O-Se bonds, from high-temperature methods; (b) intrinsic WSe_2 with pristine vdW gap interface from low-temperature VT process. It can be observed from (a) that the interface bonds form new energy bands, which act as localized trap states. It can also be seen that the original conduction and valence bands (E_c and E_v) suffer from severe distortion. Both phenomena can significantly degrade carrier mobility.

C. Grain Boundaries

1. Introduction – Formation of Grain Boundaries in Growth

The development of Chemical Vapor Deposition (CVD) technology in the synthesis of large-area monolayer MoS_2 enables the possibility of fabricating entire digital circuits and systems on MoS_2. However, the current synthesis techniques can only grow individual MoS_2 domains or polycrystalline MoS_2 films on dilectric substrates. **[180]–[184], [296]**. If grain boundaries exist in the channel of a FET, the imperfection sites will induce extra scattering, thereby causing varations in the device performance. Hence, grain boundary effects on the electrical properties of MoS_2 film can not be ignored.

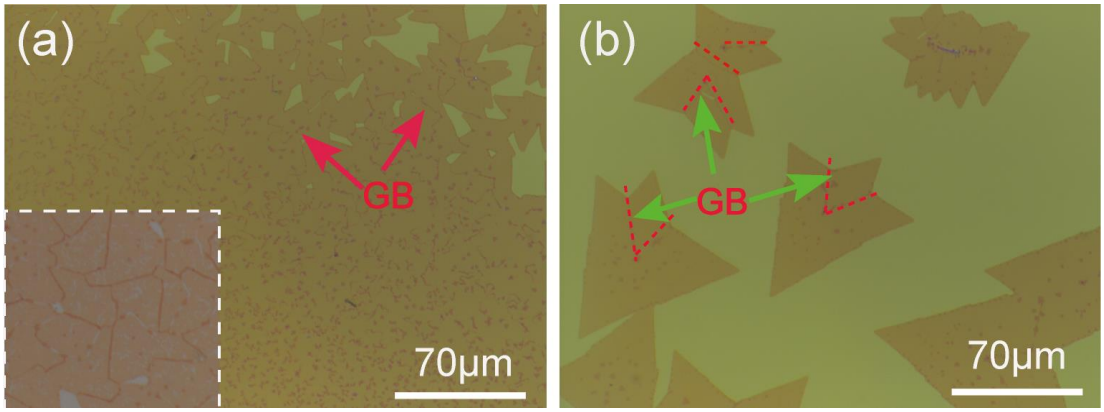


Figure 88. Photos of grain boundaries in monolayer CVD MoS_2.

(a) Low magnification optical microscope image of the of monolayer MoS_2 film synthesized by CVD. Dark dots and lines indicate the grain boundaries which are indicated by the red arrows. Inset shows a large magnification optical microscope image. Dark lines are stacked grain boundaries. (b) High magnification optical microscope image of the individual domains. The grain boundaries are illustrated by the red dash lines.

Although the effects of grain boundaries on the performance of CVD MoS_2-FETs have been noticed in few works **[182], [296], [297]**, there is a lack of comprehensive study of grain boundary effects on the carrier transport in CVD monolayer MoS_2. This section will be helpful in optimizing the design and performance of MoS_2 for nanoscale electronic and optoelectronic devices. It is also critical for optimizing the CVD process for emerging 2D materials including MoS_2. In this part, by ab-initio theoretical calculations with carefully designed experiments, we report a systematic approach to understand grain boundary effects on the performance of monolayer MoS_2-FETs on CVD synthesized high quality samples.

2. DFT-NEGF Simulation of Grain Boundaries

Density functional theory (DFT) and Non-equilibrium Green's Function (NEGF) simulation are employed to reveal the physics of the MoS_2 grain boundaries (**Figure 89**). The GB system is constructed as illustrated in **Figure 89a**. Three mechanisms for current degradation are identified and summarized (as shown in **Figure 89b**) – I. *Gap states*, II. *orbital vanishing* and III. *Potential Fluctuation*. The effects of the three mechanisms can be explained by the transmission spectrum **(Figure 89c**), density of states (DOS) of GB (**Figure 89d)** and wave functions of gap states and conduction band states (**Figure 89e,f**, respectively).

As shown in **Figure 89b**, *gap states* appear in the band gap of GB region. These states do not contribute to the conduction of carriers since at energy E_1 in **Figure 89b**, zero-transmission is found. As shown in **Figure 89d**, high DOS of gap states can be found at the grain boundary. Moreover, these states are localized at the grain boundary (**Figure 89e**) and hence carriers may fill into these high DOS localized states and thereby act as scattering centers that reduce the current.

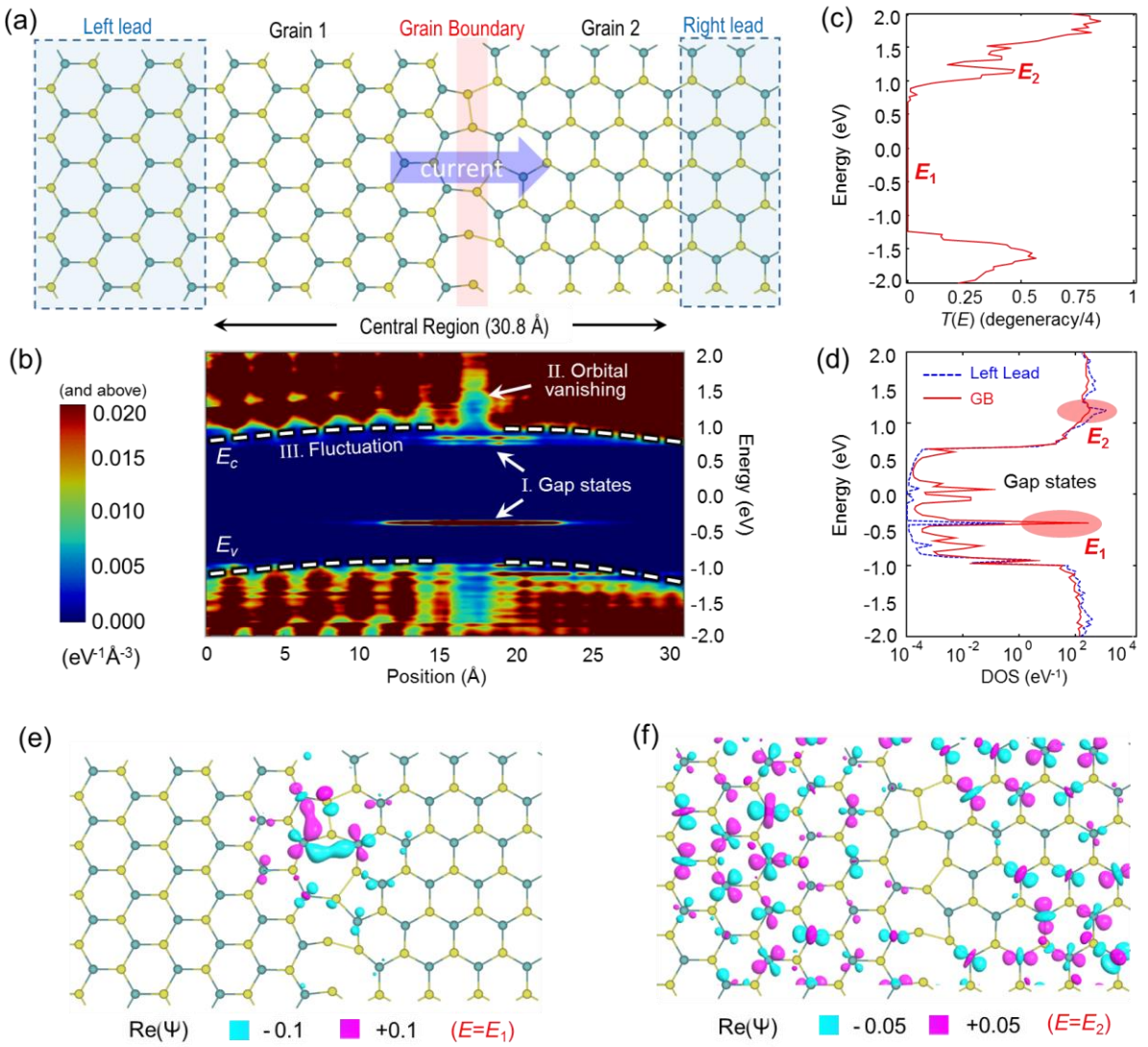


Figure 89. DFT-NEGF simulation of grain boundaries.

(a) Geometry configuration (after DFT relaxation) of two grains with a grain boundary.

(b) Local density of states (LDOS) contour along transport direction. E_c and E_v represent the conduction and valence bands, respectively. Three mechanisms for current degradation are marked by I, II and III.

(c) Transmission spectrum ($T(E)$), probability of carrier transport at different energy) across the grain boundary. E_1 and E_2 are the energy levels where gap states and orbital vanishing are happening, respectively. Gap states at E_1 do not contribute to conduction.

(d) Density of states (DOS) at the grain boundary (red) compared to DOS in the left lead (with E_c aligned), showing the gap states have high DOS.

(e) Real part (Re(ψ)) of wave function of electrons at orbitals with energy E_1 (marked in (c,d)), corresponding to gap states on the grain boundary. The blue "-0.1" and pink "+0.1" correspond to contours of different Re(ψ)). The wave functions of gap states are significantly localized at the GB.

(f) Re(ψ) of electrons at orbitals with energy E_2 (marked in (c,d)), corresponding to conduction band states,showing that no electrons are available at energy E_2 in the GB region. E_c orbitals vanish at grain boundary (mechanism II in (b)), and hence the current is degraded.

Orbital vanishing at conduction and valence band means the missing of original orbitals and states in conduction and valence bands due to defects at GB, as shown at the band edges in **Figure 89b**. It can be observed at the grain boundary in real space (**Figure 89f**), where no electron wave function can be found, which contributes to the degradation of carrier transport.

Potential Fluctuation can be indicated by the bended band diagram shown in **Figure 89b**, which is induced by the disorderly distributed charges as a result of both mechanisms I and II. The fluctuation acts as a bump/dip for carriers transporting across the GB and eventually scatters the current.

3. Grain Sizes vs. Mobility by Modeling

DFT simulations of grain boundaries yields the line density of impurities, which is then used to evaluate the impurity scattering. Grain boundaries can form between many combinations of orientations (**Figure 90a**). Here the most representative case, the grain boundary between armchair and zigzag orientations is taken as an example (**Figure 90b,c**), which shows that in general, along 1.56 nm of this grain boundary, there are 4 trap states leading to a line defect concentration of 2.56 states/nm.

Phonon scattering is always present, and limits the mobility at low defect concentration. The overall mobility in the sample is finally calculated by applying Matthiessen's rule **[298]** to both impurity and phonon scattering.

Trap states along grain boundaries of polycrystalline semiconductor act as scattering centers when charged. **Figure 91** shows the upper limit on mobility in a 2D sample as a function of the grain size, compared against published results from various growth techniques. MOCVD, CVD, and PECVD processes generally yield the highest mobilities, but require high growth temperatures, hampering integrability and reproducibility. Conversely, low temperature ALD growth gives excellent control of thickness and coverage, but suffers from low mobility due to small grain size. Sputtering is a low cost, low temperature growth process, but gives poor growth quality. MBE gives good quality of growth, but is slow and expensive.

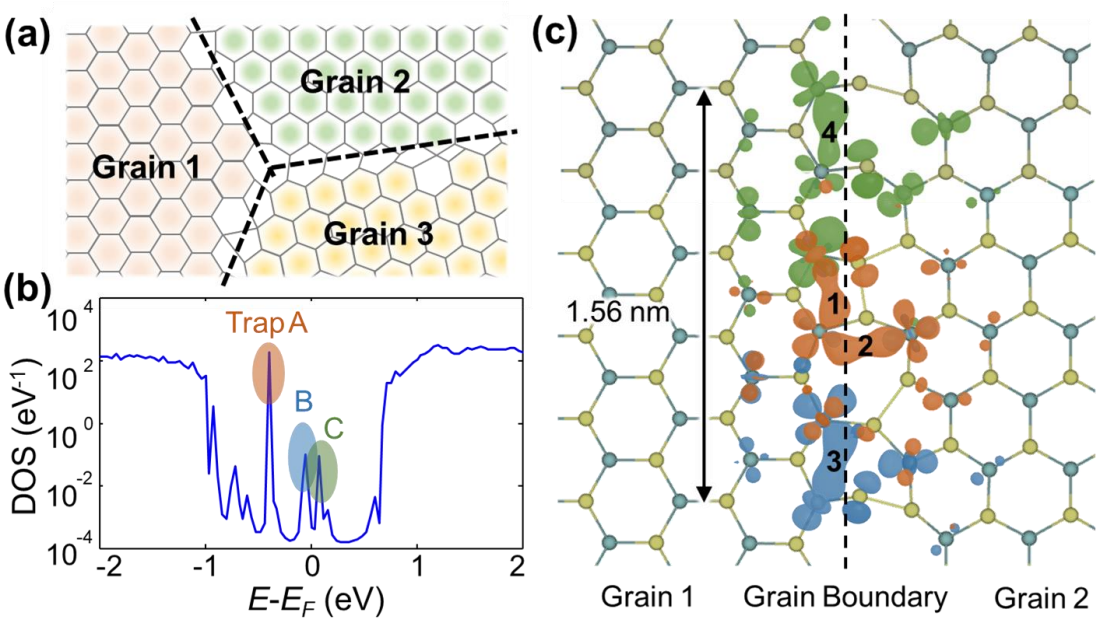


Figure 90: Analysis of trap states induced by GBs.

(a) Illustration of various grains and grain boundaries in 2D. (b) Density of states (DOS) of a grain boundary in MoS_2 between armchair and zigzag grains. Trap states (A, B, C) can be found in the band gap. (c) Wave function isosurface at Re|ψ| = 0.1 of the three trap energies shown in (b). Four large electron clouds (1-4) can be seen, which can act as impurities when full. The equivalent impurity density along a GB is 2.56/nm. The simulation was performed with Atomistix Toolkit [242].

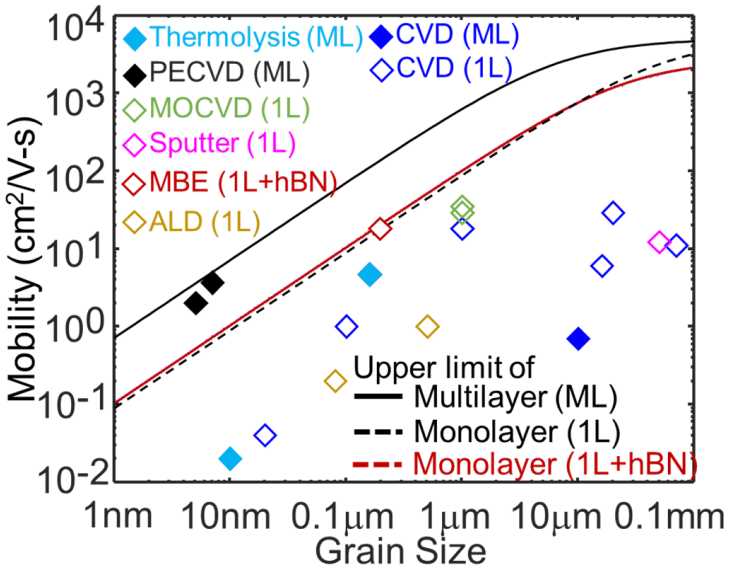


Figure 91: Mobility versus grain size.

Simulations of a monolayer (1L) and multilayered (ML) MoS_2 sample, with SiO_2 and hBN dielectrics for both gates, under an assumed mobile charge density of 2×10^{16} m^{-2}. Plot also shows mobility obtained from published data for a variety of process technologies.

4. Summary of Grain Boundaries

In summary, in this section, we report a computational study of the effects of hybrid grain boundaries on CVD synthesized monolayer MoS_2. Our results reveal that grain boundaries play a decisive role in determining the carrier mobility and performance of MoS_2-FETs. In the ON-state, if current flows across a grain boundary that is aligned perpendicular to the channel length, the current can be significantly reduced, while in the OFF-state, the effect is negligible. To understand the origin of such effects, density functional theory based ab-initio calculations are employed, and it is shown that the grain boundary effects can be explained by existence of gap states, orbital vanishing and

broadening of transmission energy barrier. This work provides useful information and guidance in understanding the nature of carrier transport in synthesized MoS_2 devices, and the developed framework can be applied to other 2D semiconductors in general, as well as in optimizing the CVD process and device design with 2D materials.

D. Quantum Dots and Superlattices

In this section, a very unique interface based on MoS_2 is studied and utilized to realize quantum dots on MoS2 with size and site control and hence design a superlattice with tunable optical gaps, which can be used in optoelectronics.

1. Introduction

Ordered arrays of quantum dots in two-dimensional (2D) materials would make promising optical materials. Recently we demonstrated a scalable, site and size controlled fabrication of quantum dots in monolayer MoS_2 and quantum dot arrays with nanometer-scale spatial density by focused electron beam irradiation induced local 2H to 1T (see **Figure 9** for crystal structures of these two phases) phase change in MoS_2 **[299]**. By designing the quantum dots in a 2D superlattice, we have shown that new energy bands are formed where the new band gap can be controlled by the size and pitch of the quantum dots in the superlattice. Here the modeling of such superlattice based on 1T and 2H MoS_2 is presented, demonstrating the tenability of the bandgaps by 1T MoS_2 quantum dots size and sites.

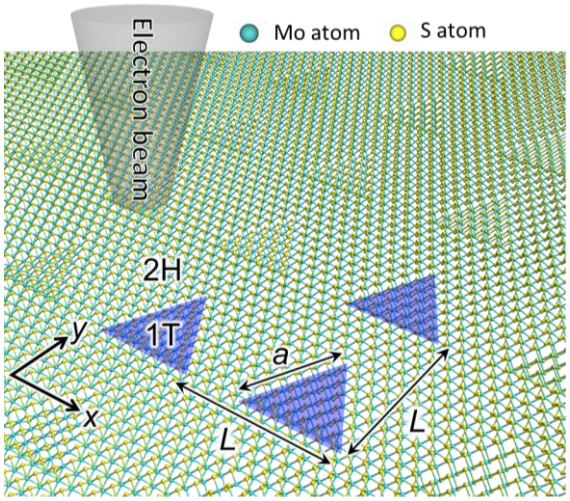


Figure 92: 1T phase quantum dot superlattice created on 2H phase MoS_2.

Schematic of electron beam irradiation on 2H (semiconducting) phase MoS_2 to trigger the transition of 1T (metallic) phase triangular MoS_2 quantum dots, where *L* is the lattice spacing (or pitch) and *a* is the side length of the 1T phase triangle.

2. 1T and 2H MoS_2

The band structures and the work functions of 1T and 2H MoS_2 were calculated via ab-initio density functional theory (DFT). Local density approximation (LDA) was adopted for the exchange correlations **[230]**, which provides consistent accuracy for band structure calculations of TMDs **[300]**. A double-ζ polarized basis set was used for expanding electronic density. The calculations were performed using Atomistix ToolKit (ATK) **[242]**. 9×9×1 k-points were sampled in the Brillouin zone. The temperature was set to be 300 K. The density mesh cut-off was 75 Rydberg and the maximum force was 0.05 eV/Å for geometry optimization (relaxation). Vacuum was added both on the top and on the bottom of the MoS_2 monolayer, to ensure that the effective potential has enough distance to decay to the vacuum level and no basis functions extend to the edge of the cell, respectively.

The band structures of 1T and 2H MoS_2 are shown in **Figure 93**. The effective masses were thus calculated based on the curvature of the dispersion curve at the extrema near the Fermi level using the classical equation:

$$m^* = \hbar^2 / k \times 1 / \left(\partial^2 E / \partial k^2 \right) \tag{12}$$

For each phase, the lowest effective mass was taken for each type of carriers (electrons and holes) for simplicity although there can be more than one extrema near the Fermi level.

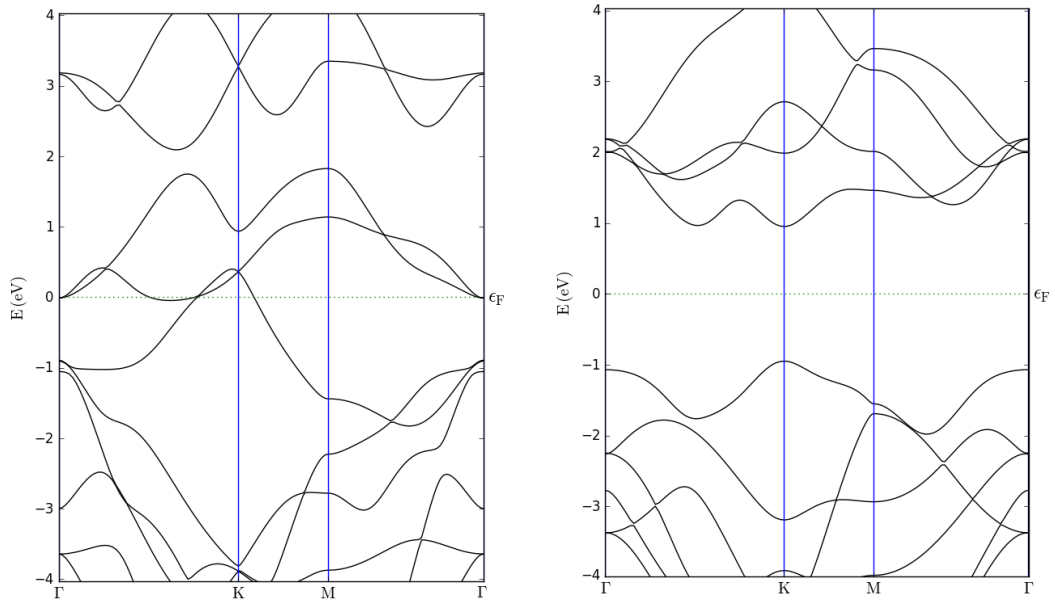


Figure 93: Calculated band structures of 1T and 2H phase MoS_2 by DFT. Left: 1T; right: 2H.

For work function calculation, an additional layer of MoS_2 atoms with basis sets but without any pseudopotential core or charge were put on top of the MoS_2 surface. The basis set orbitals can be populated in order to host a finite electron density in a region where there are no real atoms, which extends the range of the electron density into the vacuum so that it has time to decay. The effective potential is normalized to zero on the top boundary (far

away from the surface) of the unit cell by using the Dirichlet boundary condition. The work function then becomes equal to the Fermi level or chemical potential. The gradient of the potential is made to vanish on the bottom of the system by Neumann condition. The above setup provides accurate results for many crystals compared with experiments **[301]**.

3. Band structures for 1T-2H superlattice

In this sub-section, we first discuss the band structure of 1T-2H phase superlattice qualitatively, then calculate it quantitively. Please note that we do not need to assume any specific 1T-MoS_2 quantum dot size or electron/hole mass to explain the red-shifted PL. This is due to the following reasons. First off, any quantum well will always have lower ground state energy w.r.t the height of the potential well. As a result, the effective bandgap of the metallic quantum dot will be smaller w.r.t that of the surrounding semiconductor.

Moreover, because larger quantum dot has smaller ground state energy, the metallic quantum dot's bandgap always decreases with increasing size of the quantum dot. Hence, "red shift" does not depend on the specific size of the quantum dot.

Additionally, the above conclusion is independent of the specific values of the electron/hole mass. Therefore, the explanation for the red-shift does not depend on the effective mass used in the following calculations.

The derivation starts from the two-dimensional Schrödinger Equation,

$$-\frac{\hbar^2}{2m^*}\Delta_{\boldsymbol{r}}\psi(\boldsymbol{r})+U(\boldsymbol{r})\psi(\boldsymbol{r})=\varepsilon\psi(\boldsymbol{r}) \tag{13}$$

where m^* is the effective mass (for 2H phase MoS_2 electron $m^*_{e,2H}=0.54m_0$ or hole $m^*_{h,2H}=0.44m_0$, for 1T phase MoS_2 electron $m^*_{e,1T}=0.29m_0$ or hole $m^*_{h,1T}=0.23m_0$), $\Delta_{\boldsymbol{r}}=\nabla^2_{\boldsymbol{r}}=\left(\frac{\partial}{\partial x}+\frac{\partial}{\partial y}\right)^2$ is the Laplacian operator, $\psi(\boldsymbol{r})$ is the wave function at vector

$\boldsymbol{r} = x\hat{\boldsymbol{x}} + y\hat{\boldsymbol{y}}$, ε is the eigenvalue, and $U(\boldsymbol{r})$ is the potential energy at $\boldsymbol{r}$,

$$U(\boldsymbol{r}) = \begin{cases} 0 & (\boldsymbol{r}\ in\ QW) \\ U_e\ or\ U_h & (\boldsymbol{r}\ out\ of\ QW) \end{cases} \tag{14}$$

where U_e and U_h are the potential barrier heights of electrons and holes, respectively. According to the DFT simulations, $U_e = 0.915\ \text{eV}$ and $U_h = -0.905\ \text{eV}$. The $U(\boldsymbol{r})$ is defined by the triangle quantum dot structure as shown in **Figure 94a** and illustrated in **Figure 94b**.

$\psi(\boldsymbol{r})$ is a periodic function, and the boundary conditions can be expressed as:

$$\psi(\boldsymbol{r}) = \psi(\boldsymbol{r})\exp\left(i\boldsymbol{k}\bullet\left(n_x L\hat{\boldsymbol{x}} + n_y L\hat{\boldsymbol{y}}\right)\right),\ n_{x(y)} = 0,\ 1,\ 2,\ \ldots \tag{15}$$

where L is the period of the super lattice, $\hat{\boldsymbol{x}}$ and $\hat{\boldsymbol{y}}$ are the unit basis, and $\boldsymbol{k} = k_x\hat{\boldsymbol{x}} + k_y\hat{\boldsymbol{y}}$ is the wave vector.

The problem can be discretized. First let the real space (x-y plane) be sampled by $N \times N$ points, by assuming:

$$\boldsymbol{r} = x\hat{\boldsymbol{x}} + y\hat{\boldsymbol{y}} = \frac{n_x}{N}L\hat{\boldsymbol{x}} + \frac{n_y}{N}L\hat{\boldsymbol{y}};\ n_x, n_y = 1, 2, \ldots, N \tag{16}$$

For convenience, we denote $U(\boldsymbol{r})$ and $\psi(\boldsymbol{r})$ as $U(n_x, n_y)$ and $\psi(n_x, n_y)$.

Assume an $N^2 \times 1$ matrix Φ is in the form of:

$$\Phi = \begin{bmatrix} \Phi_1 \\ \Phi_2 \\ \vdots \\ \Phi_{N^2-1} \\ \Phi_{N^2} \end{bmatrix} = \begin{bmatrix} \left[\psi(1,1) \quad \psi(2,1) \ldots \psi(N-1,1) \quad \psi(N,1)\right]^T \\ \left[\psi(1,2) \quad \psi(2,2) \ldots \psi(N-1,2) \quad \psi(N,2)\right]^T \\ \vdots \\ \left[\psi(1,N) \quad \psi(2,N) \ldots \psi(N-1,N) \quad \psi(N,N)\right]^T \end{bmatrix} \tag{17}$$

The Schrödinger Equation can then be discretized as $\mathrm{H}\Phi = \mathrm{E}\Phi$. Here $\mathrm{H} = \mathrm{H}_0 + \mathrm{U}$ is the Hamiltonian matrix. Then,

$$\mathrm{H}_0\Phi+\mathrm{U}\Phi=-\frac{\hbar^2}{2m^*}\left[\Delta_r\right]\Phi+\mathrm{U}\Phi=\mathrm{E}\Phi \tag{18}$$

where $\mathrm{H}_0=-\frac{\hbar^2}{2m^*}\left[\Delta_r\right]$, $\left[\Delta_r\right]$ is the Laplacian matrix, U is an $N^2\times N^2$ matrix:

$$\mathrm{U}=diag\left(\begin{bmatrix}\mathrm{U}_1\\ \mathrm{U}_2\\ \vdots\\ \mathrm{U}_{N^2-1}\\ \mathrm{U}_{N^2}\end{bmatrix}\right)=diag\left(\begin{bmatrix}\left[U(1,1)\,U(2,1)\ldots U(N-1,1)\,U(N,1)\right]^T\\ \left[U(1,2)\,U(2,2)\ldots U(N-1,2)\,U(N,2)\right]^T\\ \vdots\\ \left[U(1,N)\,U(2,N)\ldots U(N-1,N)\,U(N,N)\right]^T\end{bmatrix}\right) \tag{19}$$

and E is an $N^2\times N^2$ matrix,

$$\mathrm{E}=diag\left(\begin{bmatrix}E_1\\ E_2\\ \vdots\\ E_{N^2-1}\\ E_{N^2}\end{bmatrix}\right) \tag{20}$$

where $E_1,E_2,...,E_{N^2}$ are the energy levels.

The function $diag(V_{M\times1})$ represents a square diagonal matrix with the elements of $M\times1$ matrix (or vector) $V_{M\times1}$ on the main diagonal.

Now the form of vector $\left[\Delta_r\right]\Phi$ should be derived. Let vector $\Theta=\left[\Delta_r\right]\Phi$ and,

$$\Theta=\begin{bmatrix}\Theta_1\\ \Theta_2\\ \vdots\\ \Theta_{N^2-1}\\ \Theta_{N^2}\end{bmatrix}=\begin{bmatrix}\left[\theta(1,1)\,\theta(2,1)\ldots\theta(N-1,1)\,\theta(N,1)\right]^T\\ \left[\theta(1,2)\,\theta(2,2)\ldots\theta(N-1,2)\,\theta(N,2)\right]^T\\ \vdots\\ \left[\theta(1,N)\,\theta(2,N)\ldots\theta(N-1,N)\,\theta(N,N)\right]^T\end{bmatrix} \tag{21}$$

Then,

$$\theta\left(n_x,n_y\right)=\left(\frac{1}{L/N}\right)^2\begin{bmatrix}\psi\left(n_x+1,n_y\right)+\psi\left(n_x-1,n_y\right)\\+\psi\left(n_x,n_y+1\right)+\psi\left(n_x,n_y-1\right)-4\psi\left(n_x,n_x\right)\end{bmatrix} \tag{22}$$

$$\Theta=\left[\Delta_r\right]\Phi=\left(\frac{1}{L/N}\right)^2\left(\mathrm{A}\Phi+\mathrm{B}\Phi+\mathrm{C}\Phi+\mathrm{D}\Phi-4\mathrm{I}\Phi\right) \tag{23}$$

where I is the elemental matrix.

Using the boundary conditions,

$$\Phi=\Phi\exp\left(i\boldsymbol{k}\bullet\left(n_xL\hat{\boldsymbol{x}}+n_yL\hat{\boldsymbol{y}}\right)\right),m_{x(y)}=0,1,2,\ldots \tag{24}$$

One can derive matrices A, B, C and D,

$$\mathrm{A}=\begin{bmatrix}\mathrm{A}_0 & & & \\ & \mathrm{A}_0 & & \\ & & \ddots & \\ & & & \mathrm{A}_0\end{bmatrix}_{N^2\times N^2},\mathrm{B}=\begin{bmatrix}\mathrm{B}_0 & & & \\ & \mathrm{B}_0 & & \\ & & \ddots & \\ & & & \mathrm{B}_0\end{bmatrix}_{N^2\times N^2} \tag{25}$$

where,

$$\mathrm{A}_0=\begin{bmatrix}0 & 1 & & & \\ & \ddots & \ddots & & \\ & & \ddots & \ddots & \\ & & & \ddots & 1\\ e^{ik_xL} & & & & 0\end{bmatrix}_{N\times N},\mathrm{B}_0=\begin{bmatrix}0 & & & & e^{-ik_xL}\\ 1 & \ddots & & & \\ & \ddots & \ddots & & \\ & & \ddots & \ddots & \\ & & & 1 & 0\end{bmatrix}_{N\times N} \tag{26}$$

and,

$$\mathrm{C}=\begin{bmatrix}0 & 0\\ \mathrm{C}_0 & 0\end{bmatrix}_{N^2\times N^2},\mathrm{D}=\begin{bmatrix}0 & \mathrm{D}_0\\ 0 & 0\end{bmatrix}_{N^2\times N^2} \tag{27}$$

where,

$$\mathrm{C}_0=\begin{bmatrix}e^{ik_xL} & & & \\ & \ddots & & \\ & & \ddots & \\ & & & e^{ik_xL}\end{bmatrix}_{N\times N},\mathrm{D}_0=\begin{bmatrix}-e^{ik_xL} & & & \\ & \ddots & & \\ & & \ddots & \\ & & & -e^{ik_xL}\end{bmatrix}_{N\times N} \tag{28}$$

The eigenvalues solved from the Hamiltonian matrix H are the energy levels $E_1, E_2, ..., E_{N^2}$, and the eigenvectors $\Phi^{E1}, \Phi^{E2}, \Phi^{E3}, \ldots, \Phi^{EN^2}$ solved from H are the wave functions. The Φ^{E1}, Φ^{E2} and Φ^{E3} are plotted in **Figure 94c-e**. The E_1 and E_1 *vs. k*, as function of *a*, are plotted in **Figure 95**. The E_1 and E_1 *vs. k* as function of *L* are plotted in **Figure 96**.

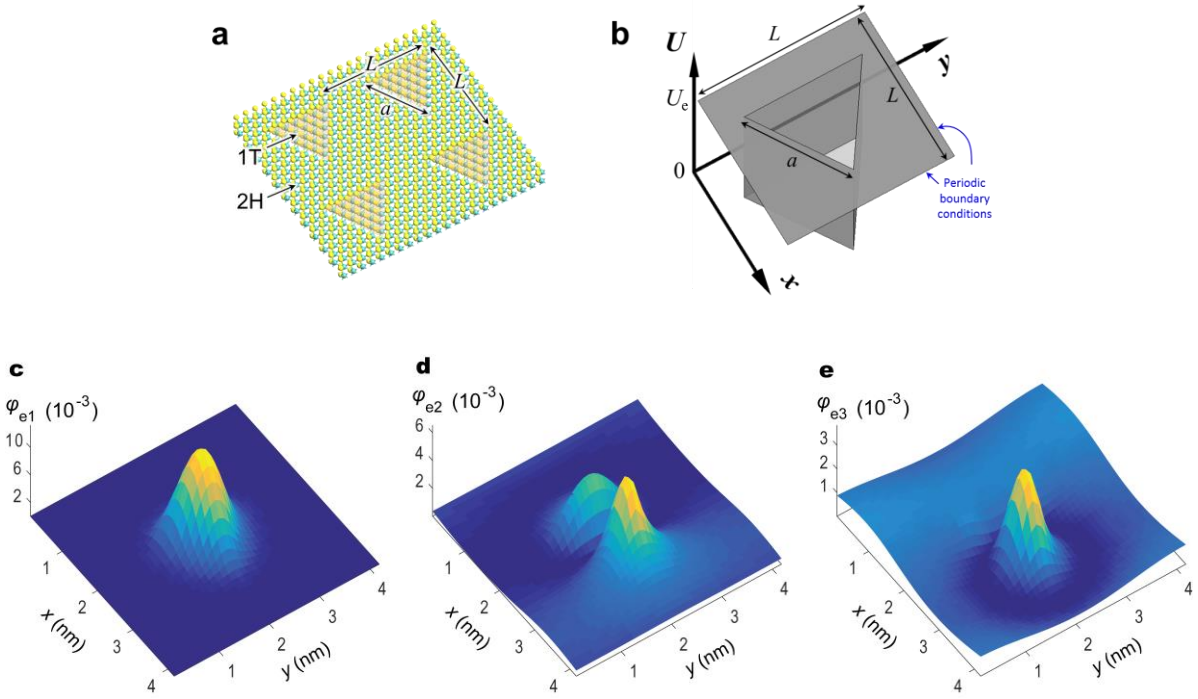


Figure 94: Schamatics and wave functions of 1T-2H MoS_2 superlattice.

(A) Schematic of the crystal structure of 1T-2H superlattice; (B) Corresponding potential profile for electrons; (C) Wave function of the first energy level at *k* = 0; (D) Wave function of the second energy level at *k* = 0; (E) Wave function of the third energy level at *k* = 0.

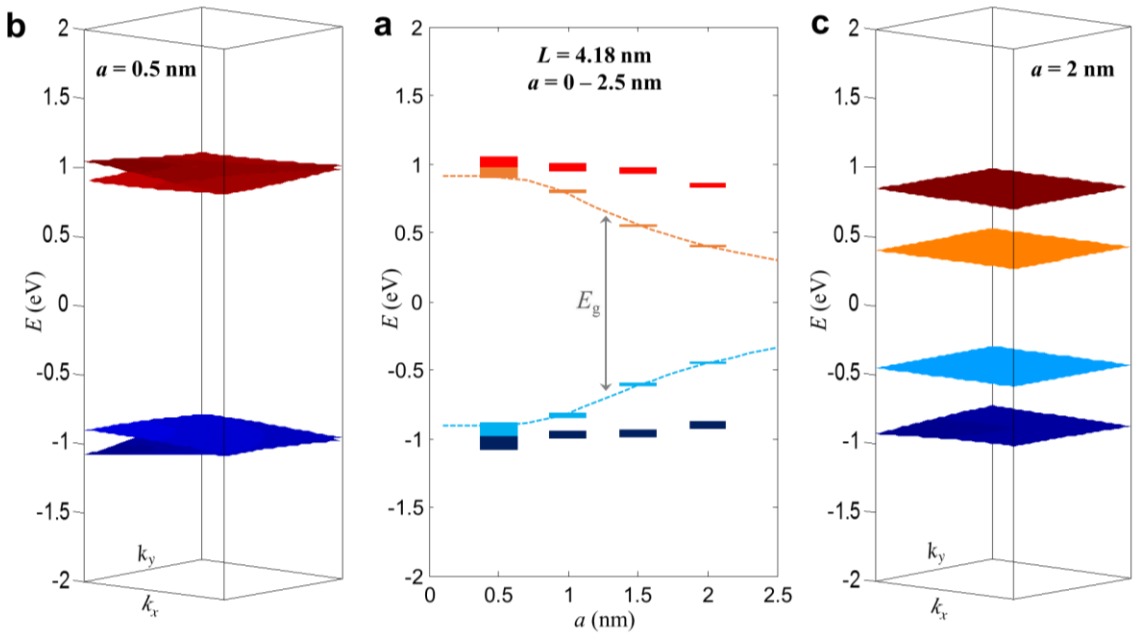


Figure 95. Superlattice band structures for different quantum well sizes.

(a), Band diagram vs. quantum well size *a* (triangle edge length) with *L* = 4.18 nm. Dashed line: band edge vs *a* for electrons and holes for MoS_2. (b), Band structure of the super lattice with *a* = 0.5 nm; (c), Band structure of the super lattice with *a* = 2 nm.

4. Experimental Demonstration and Summary

In our experiments, the 1T-2H superlattice exhibits tunable band gap from 1.81 eV to 1.42 eV without loss of photoluminescence performance **[299]**, which opens up new pathways of fabricating lasers with designed wavelengths. Our work constitutes a photoresist-free top-down method to create large-area quantum dot arrays with nanometer-scale spatial density that allow the quantum dots to interfere with each other and create artificial crystals and thereby opens up new pathways for fabricating light emitting devices with 2D materials at desired wavelengths. This research can also enable assembly of large scale quantum information systems and open up new avenues for the design of artificial 2D

materials.

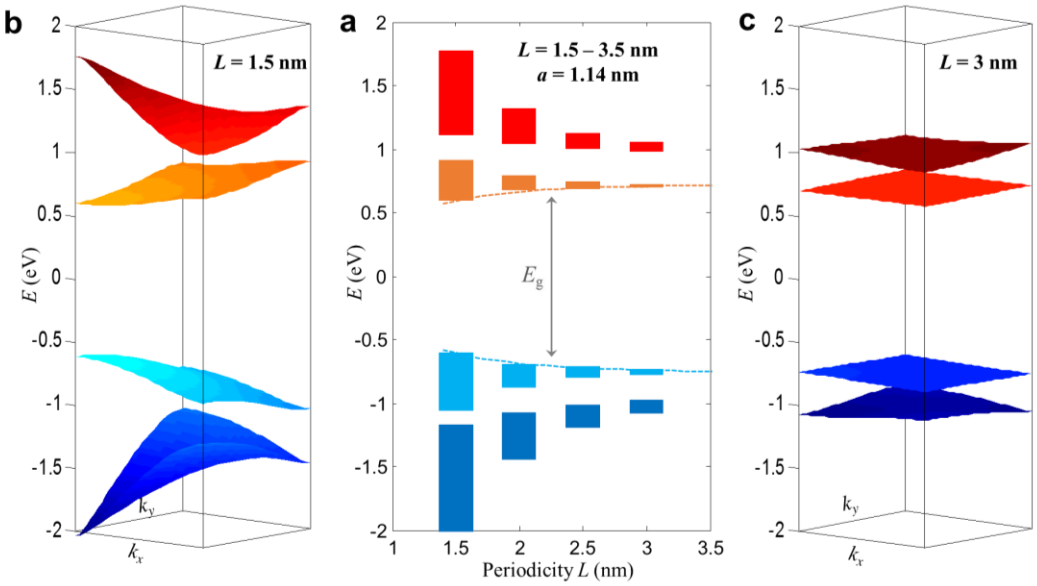


Figure 96. Superlattice band structures for varing periodicity.

(a), Band diagram vs. super lattice periodicity *L*. *a* = 1.14 nm. Dashed line: band edge vs *a*, for electrons and holes in MoS_2. (b), Band structure of the superlattice with *L* = 1.5 nm; (c), Band structure of the superlattice with *L* = 3 nm.

E. 2D Tunnel Field-Effect Transistors

1. Introduction – 2D TFET

Tunnel-FET (TFET) utilizing BTBT,**[45], [302]–[307]** is a promising candidate for achievement of sub-thermionic *SS* (**Figure 97**). The demonstration of Band-to-Band Tunnel-FETs (TFETs) based on 2D semiconducting-channel material (**Figure 98**) exhibits steep turn-on, with a minimum *SS* of 3.9 mV/dec as well as an excellent average *SS* of 31.1 mV/dec for 4 decades of drain-current at room temperature. By engineering the substrate to

employ a highly doped Germanium as source and using atomically-thin molybdenum disulphide (MoS_2) as the layered semiconducting-channel, an unique vertical heterostructure device is built, not only retaining the advantages of 2D materials but adding extra functionality, to achieve excellent electrostatics, strain-free heterointerface, low tunneling barrier, and large tunneling area in a manufacturing-friendly planar-platform.

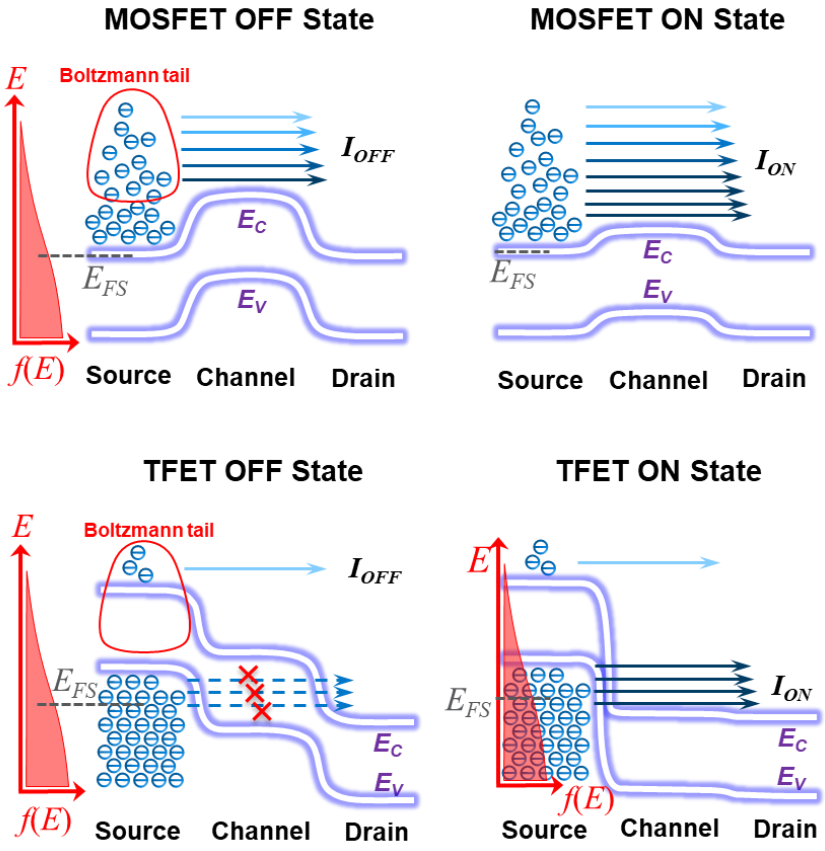


Figure 97: Mechanisms of TFET compared to that of MOSFET.

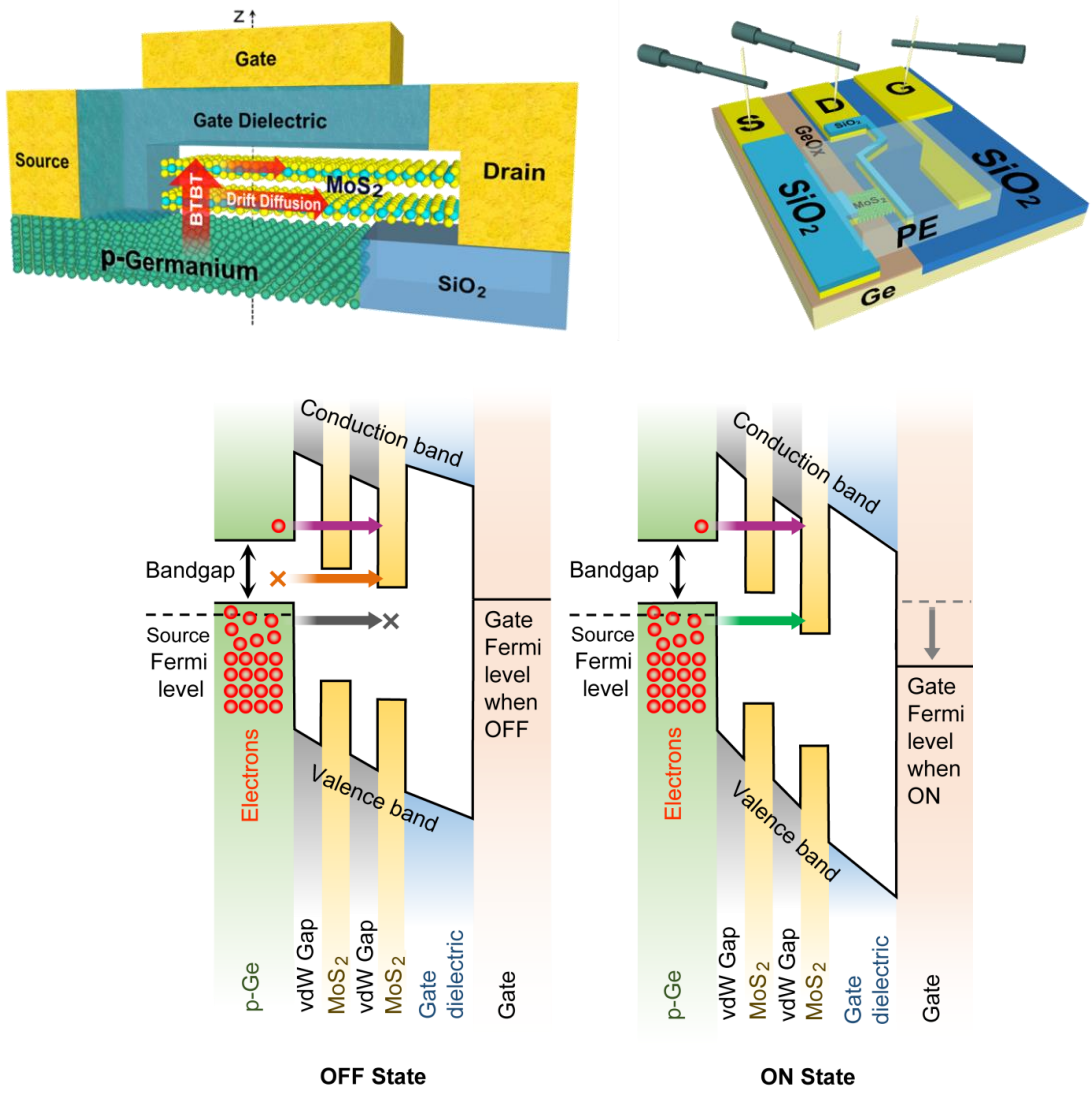


Figure 98: Schematics and working principles of 2D-TFET [9].

For the top left schematic, path for electron transport is shown by the arrows which run vertically from the Ge source to the MoS_2 and then laterally through the MoS_2 layers to the drain. As shown in the bottom schmatics, since the Ge is highly doped, the tunneling barrier height is mainly determined by the effective bandgap of MoS_2 (including van der Waals gap) while the tunneling width is determined by the MoS_2 thickness.

In this section, using DFT simulations, the band alignment at the Ge-MoS_2 3D-2D tunnel interface is studied, which proves the working principle of such junctions. In addition, another possible 3D-2D tunnel junction, the InAs-WSe_2 interface, is calculated as well, showing a promising band alignment that will work for p-type TFET.

2. 2D-3D Tunnel Interface – Computational Study

The band alignment at the Ge-MoS_2 interface is calculated via ab-initio density functional theory. The interface in the unit cell is periodical in *x* and *y* direction and separated by vacuum in *z* direction (20 Å each side), as shown in **Figure 99a,b** and **Figure 100a,b**. The interface contains a Ge (InAs) slab with (100) surface (oxidized) and a tri-layer MoS_2 (WSe_2) slab on top. The Ge (InAs) slab thickness is chosen to be 60 (75) Å, since any thickness below this point gives 0.05 eV higher band gap compared to bulk Ge, due to quantum confinement effect. To model the p-doped Ge (n-doped InAs), atomic compensation charge (molar fraction 0.1%) is applied to Ge (InAs) atoms. The germanium oxide layer is modeled by adding a few layers of GeO_x ($x \approx 1.6 - 2$) at the Ge surface (*x* depends on which layer of Ge has been take into account to calculate the ratio). By DFT evaluations, it is found that this oxide layer does not affect the band structure of Ge beneath (preserves the properties of bulk Ge). All atoms on the on the Ge (InAs) surfaces are terminated by H atoms, if not saturated.

The calculations are performed using Atomistix ToolKit (ATK) **[242]**. Meta Generalized Gradient Approximation (Meta-GGA) **[308]** is adopted for the exchange correlations. Hartwigsen-Goedecker-Hutter basis set is used for expanding electronic density. This configuration was found to be able to reproduce the experimental band gaps of both Ge and MoS_2. 3×6×1 k-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 150 Rydberg and the maximum force is 0.05 eV/Å for

geometry optimization (relaxation).

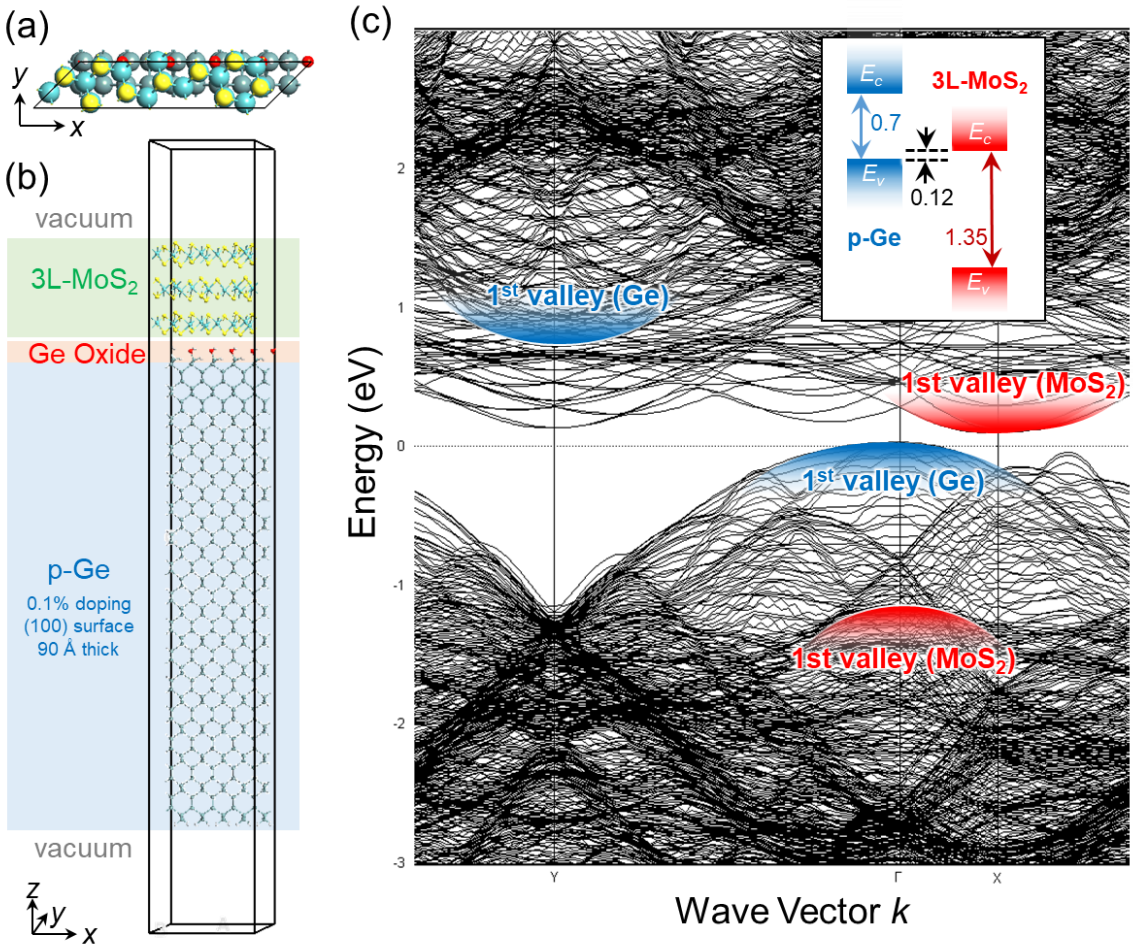


Figure 99. Simulation of Ge-MoS_2 interface.

(a) Top view and (b) side view of the Ge-MoS_2 interface unit cell. (c) band structure of the interface. The valence band maxima is chosen as energy zero. Inset shows the band alignment according to the band structure in (c).

The calculated band structures are shown in **Figure 99c** and **Figure 100c**. The first conduction and valence band valleys for MoS_2 and Ge are picked (referring to their original band structures calculated by DFT) and marked by red and blue, respectively, in **Figure 99c**. Hereafter, the band alignment is shown in **Figure 99c** inset.

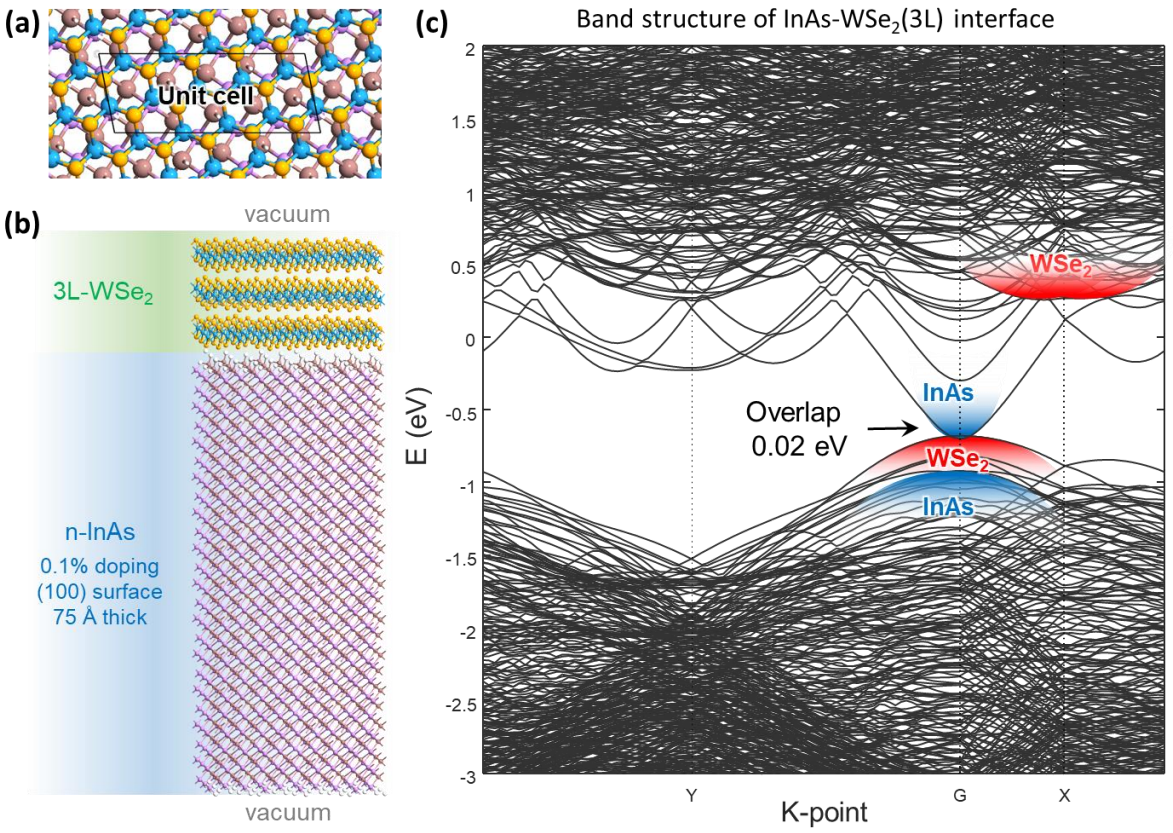


Figure 100: Simulation of InAs-WSe_2 interface.

(a) Top view and (b) side view of the InAs-WSe_2 interface unit cell. (c) band structure of the interface. The valence band maxima is chosen as energy zero.

3. Interface Engineering – Surface Reduction and Passivation

Although the MoS_2-Ge 2D-3D tunnel junction can be exploited to build the 2D channel TFETs which exhibit record subthermionic performance, however, in the first demonstration **[9]**, the drive current of such transistors is relatively low. The reason is that germanium surface is chemically active and forms native oxide (GeO_x, x=1–2) in air easily, and thus form a tunnel barrier with thickness ~ 1 nm between Ge and MoS_2, as shown in the

transmission electron microscopy (TEM) image in **Figure 101**. Due to diffusion of O_2, such oxide can even grow when MoS_2 has already covered the surface.

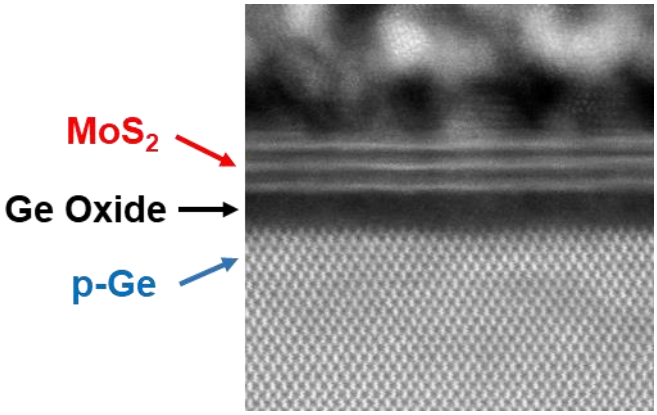


Figure 101: Cross-section TEM image of the Ge-MoS_2 tunnel interface. A germanium oxide layer can be observed between Ge and MoS_2.

Although the native germanium oxide can be removed by hydrogen halide solution (HF, HCl, HBr, etc.), however, the bare germanium surface gets oxidized by O_2 and H_2O quickly afterward. Hence, a passivation of the surface is desired to prevent the growth of GeO_x.

As shown by Collins, et al. **[309]**, citric acid, an aqueous, mild and organic acid, is highly effective for removal of GeO_x and suface passivation. In this section, the citric acid method is utilized to treat the interface of Ge-MoS_2 junctions.

First of all, XPS spectra of germanium (001 surfaces) are compared before and after treatment. As shown in **Figure 102**, after treatment, both GeO and GeO_2 peaks are eliminated, indicating the removal of the native oxide layer. Moreover, a split of Ge 3p5 peak can be observed in the inset plot. The binding energy of the new peak corresponds to Ge-C bonds **[310]**, indicating a passivation by organic atomic groups, typically -COOH groups **[309]**. The treatment process is illustrated in **Figure 103**. According to DFT

simulations, the distance between Ge and MoS_2 is reduced by half to ~0.5 nm.

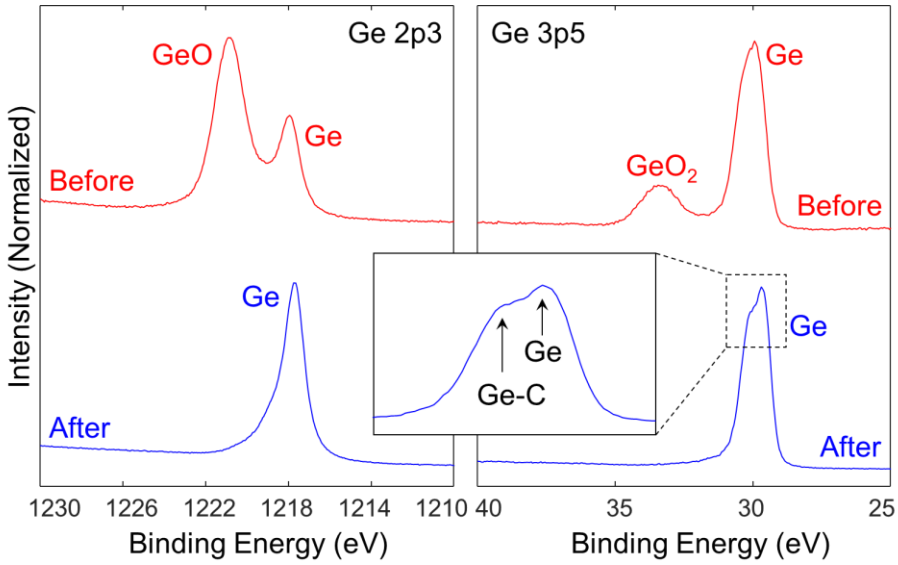


Figure 102: XPS spectra of Ge surface before and after citric acid treatment.

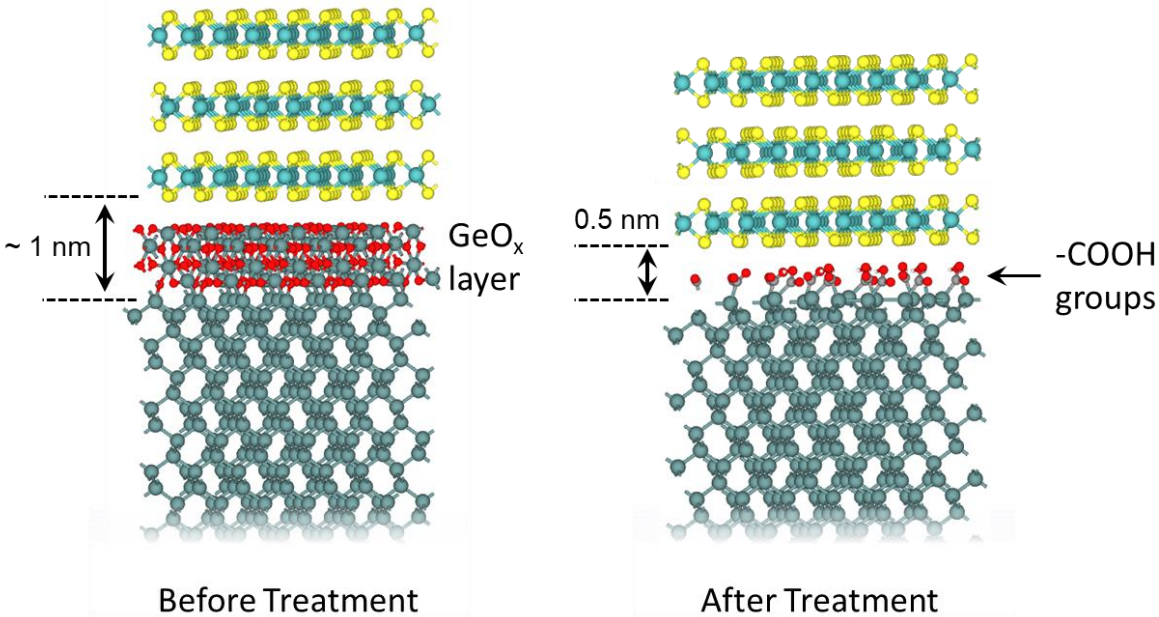


Figure 103: Atomic structures before and after reduction/passivation treatment. The structures are relaxed using DFT.

Subsequently, an experiment to compare the tunnel current through the interfaces before and after citric acid treatment is designed, illustrated in **Figure 104**. Half of a germanium substrate is treated by citric acid while the other half is left untreated. Then exfoliated MoS_2 flakes are transferred onto the surface.

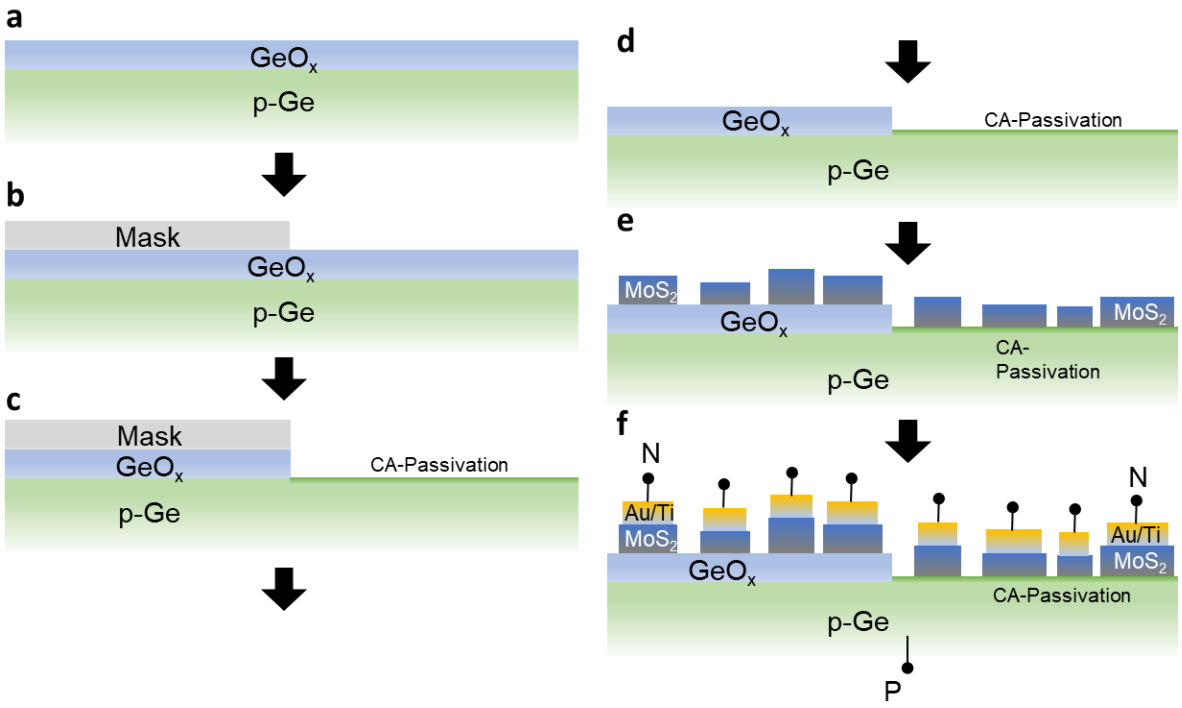


Figure 104: Fabrication flow of Ge-MoS_2 p-n junctions.

Half of the substrate is treated by citric acid (CA) to remove GeO_x and passivate.

As shown in **Figure 105**, Ti and then Au are directly deposited on the surface of MoS_2 flakes to form metal contacts.

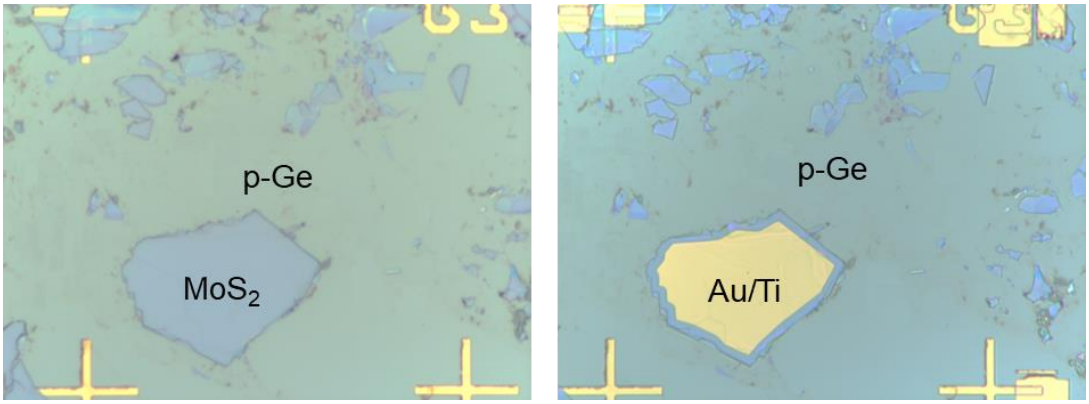


Figure 105: Photos of a Ge-MoS_2 junction before and after depositing metal contact.

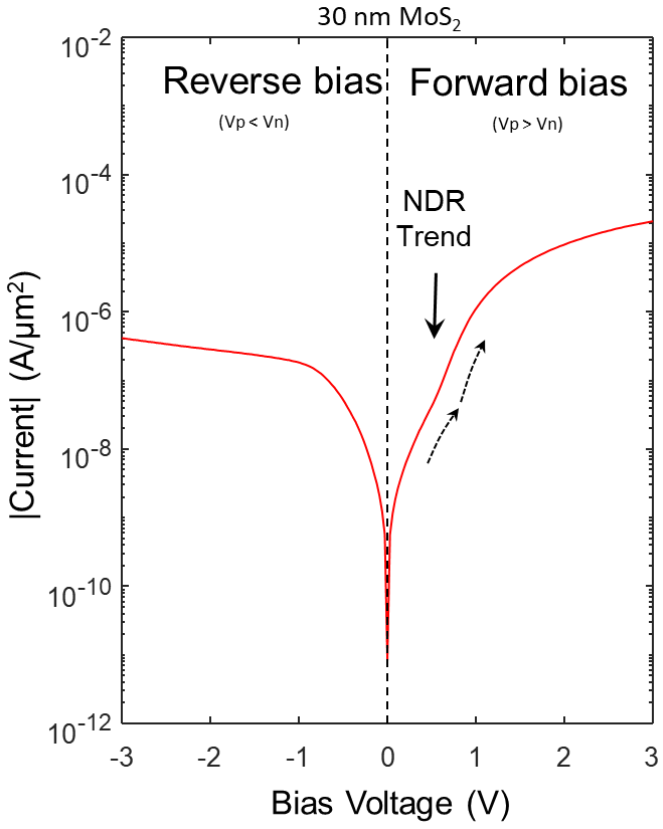


Figure 106: I-V characteristic of a Ge-MoS_2 p-n junction.

The I-V characteristic of a p-n junction consist of Ge and 30-nm-thick MoS_2 is shown in

Figure 106. A kink in the forward bias current can be observed as expected **[9]**, which indicates the junction has a trend towards negative differential resistance, a sign of tunneling **[311]**. The band diagrams to explain this I-V characteristic are shown in **Figure 107**. In the forward bias region, the increasing bias voltage reduces the tunnel window between the valence band of p-Ge and the conduction band of n-MoS_2, therefore reducing the tunnel current. When the tunnel window is totally closed, i.e. the valence band of p-Ge is lower than the conduction band of n-MoS_2, only the drift-diffusion current is left. Thus a kink is observed.

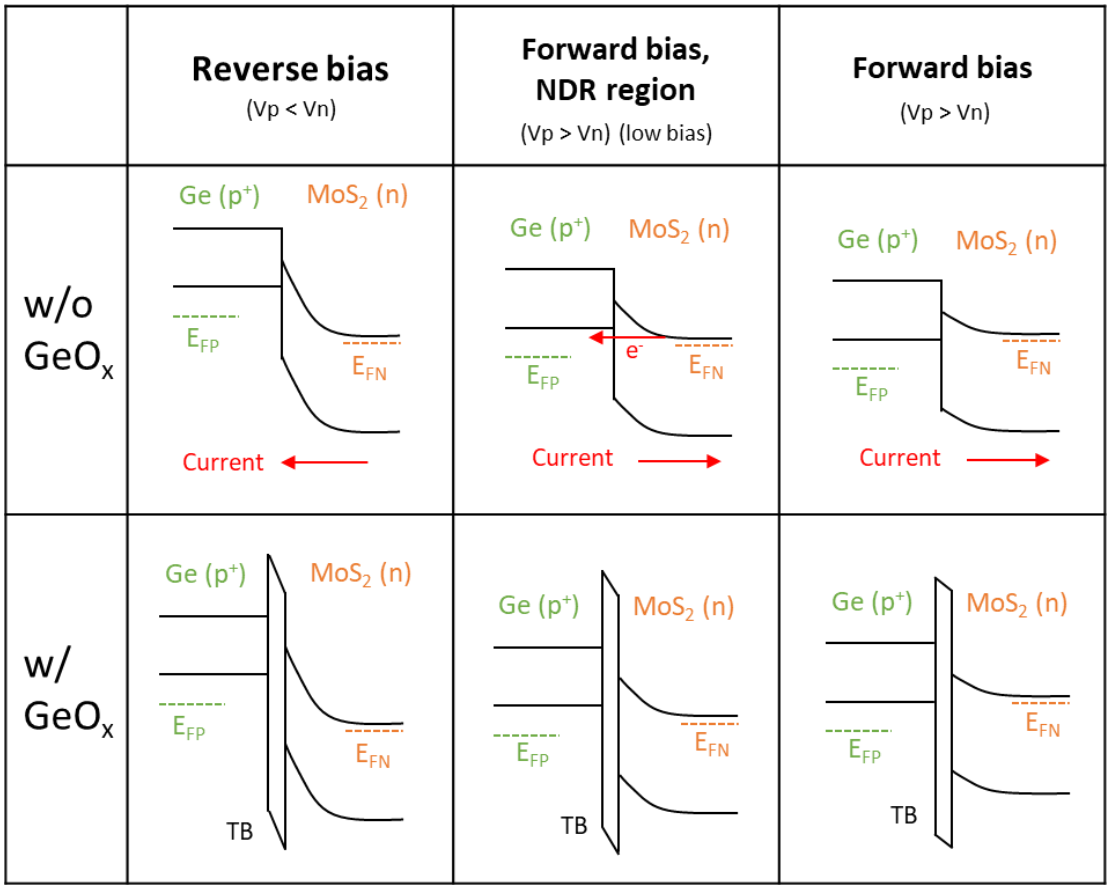


Figure 107: band diagrams of Ge-MoS_2 p-n junction at different biases.

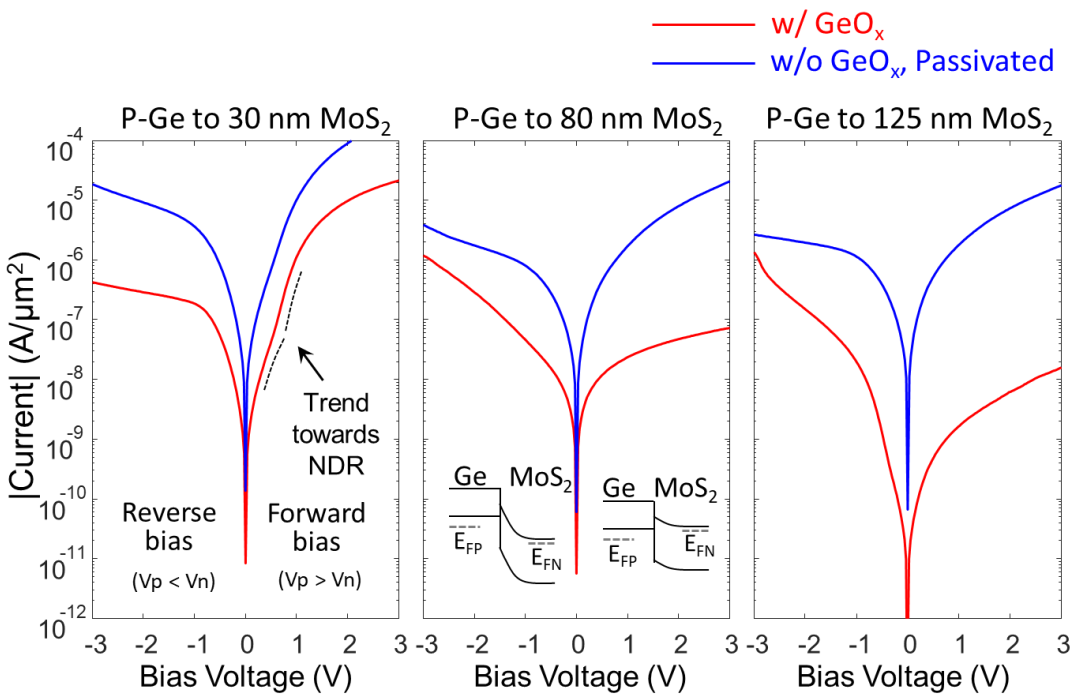


Figure 108: I-V curves of Ge-MoS_2 p-n junctions with different MoS_2 thickness.

Then the I-V characteristics are compared between before and after citric acid treatment (**Figure 108** and **Figure 109**). For different MoS_2 thicknesses, a boost in both reverse bias current and forward bias current can be observed. The improvement of current varies between one to three orders of magnitude.

As discussed previously, bare germanium surface is chemically active and forms native oxide in air easily. To evaluate the efficiency of passivation, a stability study is designed as shown in **Figure 110**. The passivated surface is left in air for one week and then MoS_2 is transferred onto the surface. It can be seen that the current through the one-week interface (purple curve) is almost the same as the fresh interface (blue curve), indicating that the passivation is effective and prevents further oxidization.

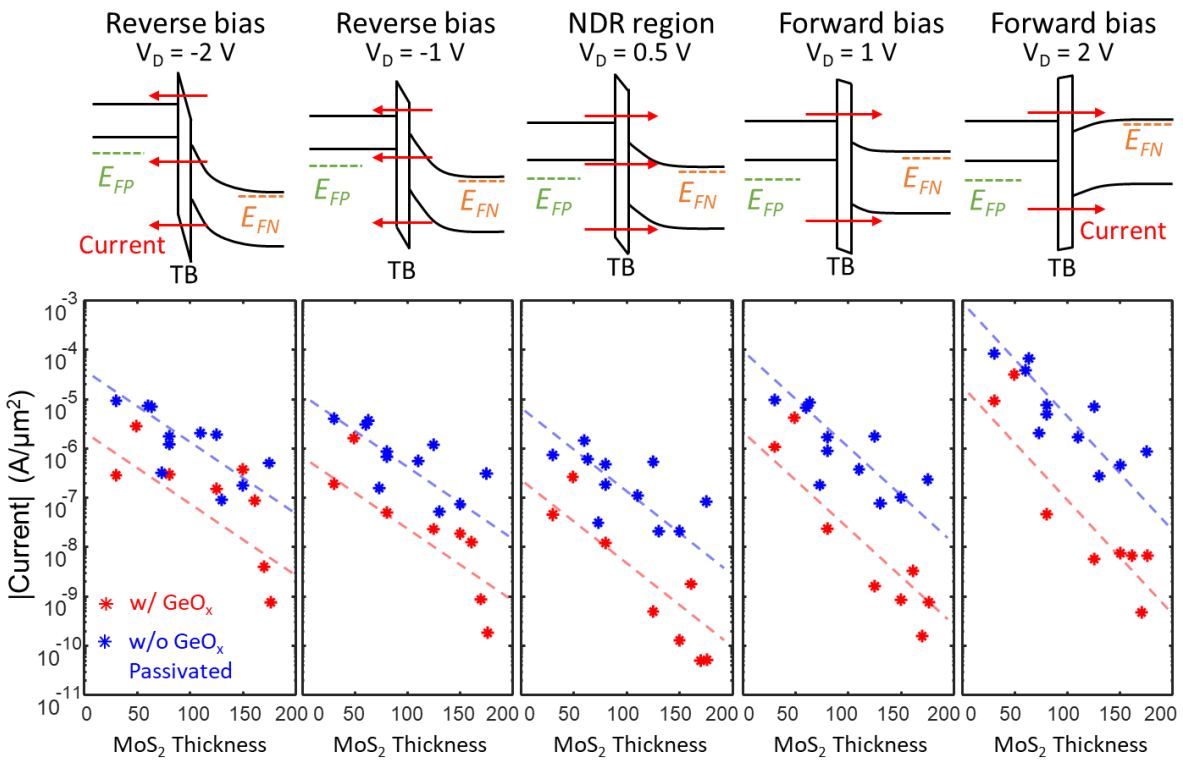


Figure 109: Currents of Ge-MoS_2 p-n junctions with different MoS_2 thickness. Top plots are the band diagrams at different bias regions. Bottom plots compare the current before and after treatment for different MoS_2 thicknesses.

Due to diffusion of O_2, germanium oxide can even grow when MoS_2 has already covered the surface. Hence, another set of experiments is designed to evaluate the stability of Ge-MoS_2 interface after covering with MoS_2, as illustrated in **Figure 111**. Similarly, the fresh Ge-MoS_2 interface is left in air for one week, and the I-V curves are compared before and after air treatment. It can be seen that after one week, the current has no degradation. Hence, the surface passivation by citric acid can also effectively prevent the oxidization of Ge after MoS_2 transfer.

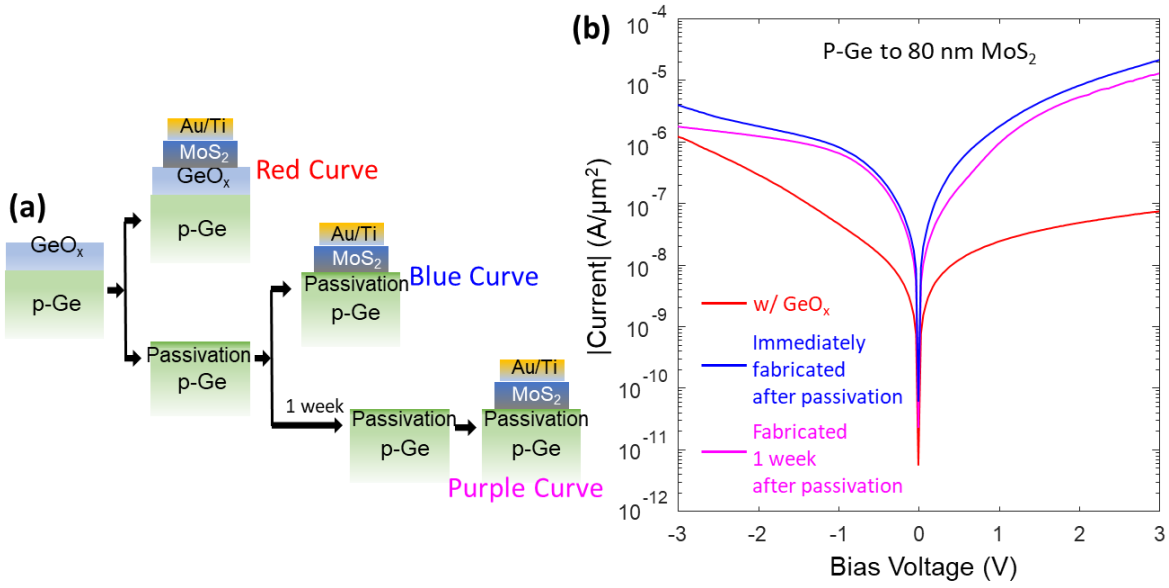


Figure 110: Stability study of passivated Ge-MoS_2 interface – part I.

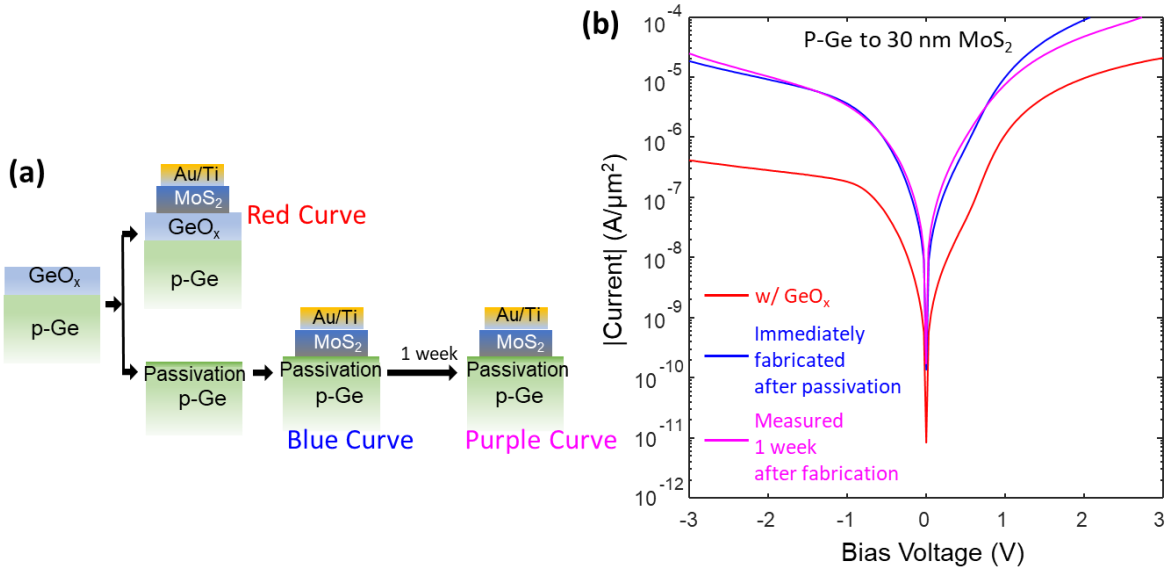


Figure 111: Stability study of passivated Ge-MoS_2 interface – part II.

In short, the interface engineering using citric acid to reduce and passivate Ge surfaces is both simple and effective. Such engineering method should be employed in 2D channel TFETs in future study.

F. Chapter Summary

In this chapter, other than the contact interface discussed in the previous chapter, various types of interfaces involving 2D materials are researched, including the interfaces between 2D semiconductors and dielectrics (substrates and gate oxides), grain boundaries – the interfaces between grains inside a 2D semiconductor plane (including both same crystallines and different crystallines), as well as the interfaces between 2D semiconductors and bulk semiconductors.

Apart from permittivity, the dielectric interface mechanisms are critical for 2D devices due to their influences on the mobility. Proper dielectric interfaces can be employed in device/process design for achieving high performance, such as combination of 2D and bulk dielectrics.

Grain boundaries play a decisive role in determining the carrier mobility and performance as well, which is mainly determined by the synthesis process. On the other hand, based on the Kronig-Penny model in quantum physics, the alternate grains of 1T and 2H phases of MoS_2 can be utilized to form artificial superlattices with various band gaps.

Finally, the interface properties are studied between 2D semiconductors and 3D semiconductors. Ge-MoS_2 and InAs-WSe_2 interfaces are two types of 2D-3D tunnel interfaces that can be employed for n-type and p-type TFETs, respectively, exploiting the advantages of both 3D bulk semiconductors (high doping) and 2D semiconductors (pristine interface). However the surfaces of the 3D bulk semiconductor need to be carefully treated to remove the native oxide as well as passivate to prevent further oxidization. Citric acid chemical treatment is found to be highly effective to reduce and passivate Ge surface, which has the potential to improve the tunnel current in Ge-MoS_2 TFETs.

V. Doping of 2D Materials

A. Introduction

Tuning the electrical properties of 2D materials through doping is necessary for various electronic and optoelectronic applications such as complementary logic as well as graphene passive devices (such as interconnects and inductors).

Various doping techniques (**Figure 113**) have been developed for graphene as well as other 2D semiconductors, such as, edge doping **[312]–[314]**, surface doping **[315]–[317]**, substrate doping **[318]** and electrostatic doping **[274], [319]**.

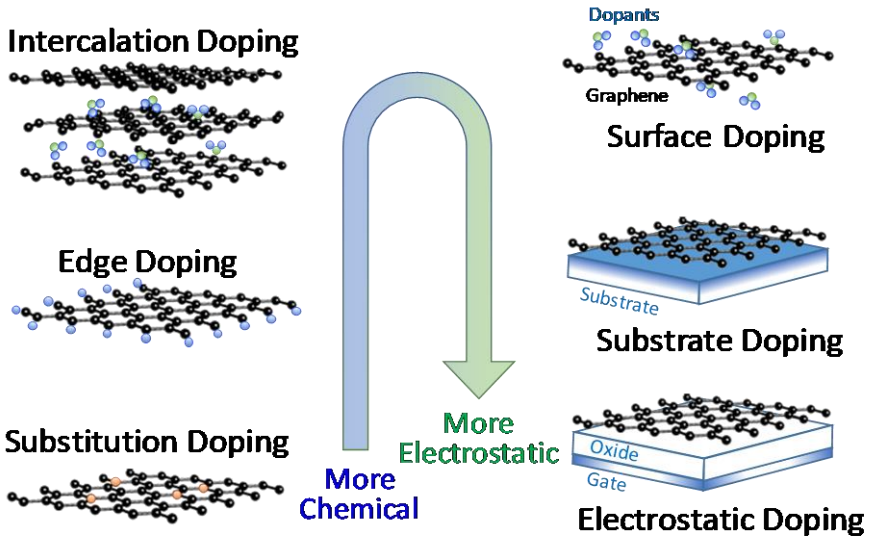


Figure 112: Various doping techniques for 2D materials.

Substitution doping **[320], [321]**, which is enabled by replacing original atoms with other dopant atoms, introduces defects in 2D plane leading to a significant degradation in its electrical properties, which can be observed by the much lower mobility and the obvious defect peaks in Raman spectra. Hence, substitution doping may not be a good option.

The surface doping method is achieved by charge exchange between 2D and adsorbed dopant atoms on the surfaces, such as H_2O vapor (p-type) and NH_3 (n-type) on graphene **[88], [322]**, as well as Br_2, I_2, K **[323], [324]** and organic molecules **[325], [326]**.

While to effectively reduce the resistance of multilayer graphene interconnects, intercalation doping technique is needed, in order to outperform Cu **[57]**. The in-plane conductivity of graphite can be increased by several tens of magnitude by intercalation doping, because doping can increase the carrier density due to charge transfer and increase the mean free path due to increased layer spacing and hence suppressed interlayer scattering **[61]**.

Both substrate doping and gate electrostatic doping are electrostatic methods and can effectively improve the charge density **[318] [327]**. The substrate can however reduce the carrier mobility due to scattering from substrate impurities and surface polar phonons **[151]**. The gate electrostatic doping, however, require extra electrodes and metal layers that induce more process steps as well as parasitics and is not a practically preferred doping technique.

Hence, considering the properties of these doping techniques, surface doping and intercalation doping are relatively stable, reliable, highly-efficient and practical. In the next sections, using Density Functional Theory (DFT), surface doping by noble metal atoms and nano-particles such as Ag and Pt have been shown to be a reliable doping method for graphene and MoS_2. The studies of intercalation doping of multilayer graphene using Bromine and $FeCl_3$ are also presented.

B. Surface Doping

Here I present two computational investigations of the doping effect on 2D materials, by surface dopants.

1. Surface Doping using Metallic Atoms

In this part, we explore the doping of graphene by metal atoms on graphene surfaces. Using density function theory, the band structures and the partial densities of states of Ag-doped graphene and Ni-doped graphene are calculated. The results show that Ag atoms can dope graphene n-type, which can increase the conductance of graphene **[10]**. However, Ni cannot dope graphene and can distort the *E-k* of graphene especially in the valence bands, which may result in the reduction of hole mobility. Hence, Ag dopants are suggested to be applied to graphene transparent electrodes to increase conductance.

Graphene, which is a thermodynamically stable and thinnest 2D material, consists of a single layer of *sp2*-hybridized carbon atoms. It is a zero bandgap semiconductor and because of its unique (linear *E-k*) band structure, graphene has zero effective mass for both electrons and holes and extremely high carrier mobility exceeding 40,000 cm^2 /V.s at room temperature on SiO_2 substrate. Moreover, graphene is a highly flexible material with high transparency, which makes it an excellent alternative to Indium Tin Oxide as a transparent electrode for light emitting diodes, solar cells, touchpad displays, and memory devices.

However, currently the conductance of intrinsic graphene electrode is not compatible with that of compound transparent electrodes. Hence, the improvement of the conductance of graphene electrode is crucial for application of graphene in photovoltaics. Doping of graphene is an effective way to increase the electron density, and improve the electrical conductivity. Without affecting the transparency of graphene electrode, surface chemical doping is the favorable method to dope graphene.

Hence, in this part, the chemical doping of graphene by metal atoms on graphene surfaces is studied using density function theory (DFT). By evaluating the band structures (*E-k*) and the partial densities of states (PDOS) of Ag-doped graphene and Ni-doped

graphene, we show that Ag is more suitable for doping graphene than Ni.

Since DFT only utilizes periodic boundary conditions, we chose interface unit cells that are periodical in *x* and *y* direction and separated by vacuum in z direction, as shown in **Figure 113**. The unit cell contains a monolayer graphene as well as a metal particle on the surface. All the atoms are allowed to relax.

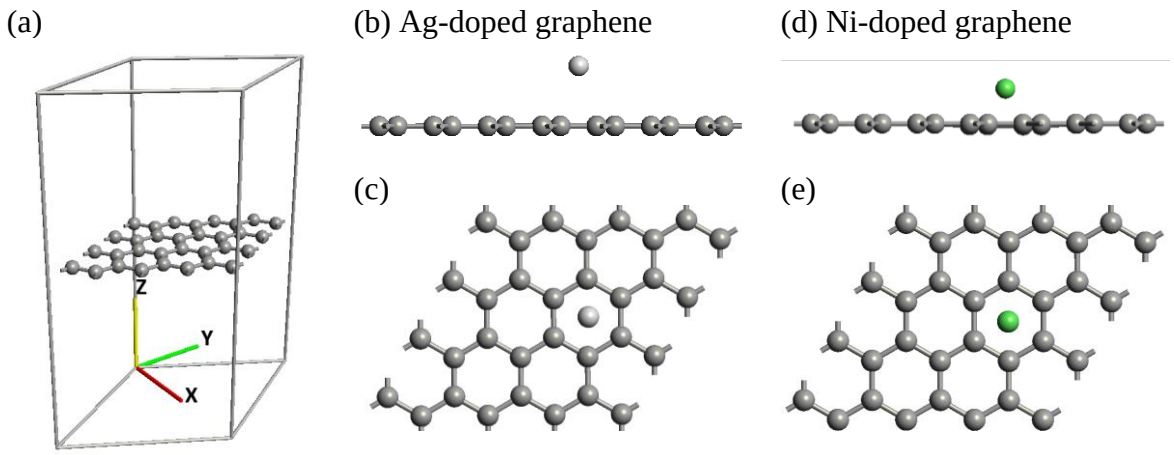


Figure 113: Crystal structures of graphene with surface doping.

(a) 3D view of unit cell with intrinsic graphene. (b) side view and (c) top view of relaxed Ag-doped graphene. (d) side view and (e) top view of relaxed Ni-doped graphene.

Numerical DFT calculations are performed using Atomistix ToolKit **[242]**. Local Density Approximation **[230]** is used for the exchange correlation potential. A double-ζ polarized basis set is used for expanding the electronic density. K-point samplings in the Brillouin zone is 8×8×1. Other parameters are density mesh cut-off =100 Ry and maximum force =0.05eV/Å for relaxation.

The *E-k* of intrinsic graphene, Ag-doped graphene and Ni-doped graphene are shown in

Figure 114. In **Figure 114b** (Ag-doped graphene), the Fermi level is shifted towards the conduction band, compared with that of **Figure 114a** (intrinsic graphene). Hence, Ag, with a dose of 3% molar fraction, can dope graphene with an n-type Fermi potential of 0.51 eV. While in **Figure 114c** (Ni-doped graphene), the Fermi level remains at the dirac point of graphene, indicating no doping effect. However, in Ni-doped graphene, the E-k of valence band is distorted. Such distortion induces localized states, which can act as scattering centers that reduce the hole mobility. On the other hand, the original valence bands are flatten due to the distortion, resulting in the increase of hole effective mass, and thus, the reduction of mobility.

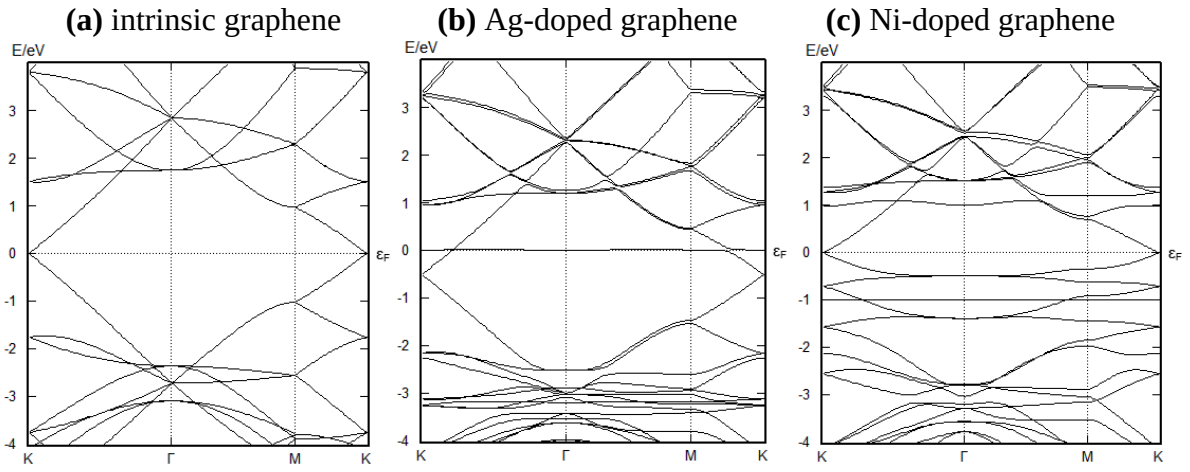


Figure 114: Band structures of doped graphene.

***E-k* of (a) intrinsic graphene, (b) Ag-doped graphene and (c) Ni-doped graphene. Ag-doped graphene is n-type. Ni-doped graphene shows no doping effect but distortion of E-k in valence bands.**

The PDOS of intrinsic graphene, Ag-doped graphene and Ni-doped graphene are shown in **Fig. 3**. Ag-doped graphene shows an n-type PDOS (**Fig. 3(b)**), while Ni-doped graphene

is still intrinsic (**Fig. 2(c)**). Moreover, localized states are found in valence bands.

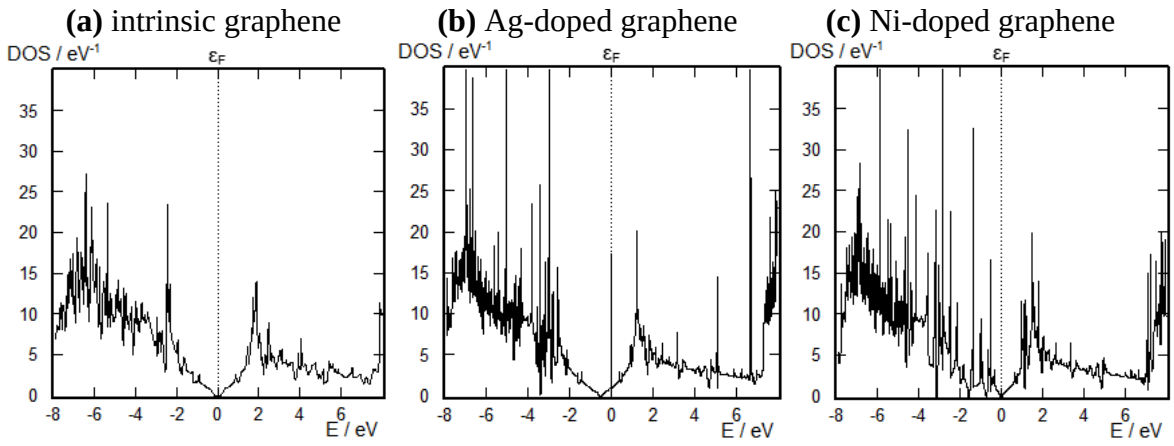


Figure 115: PDOS of graphene part in doped graphene systems.

PDOS of (a) intrinsic graphene, (b) Ag-doped graphene and (c) Ni-doped graphene. Ag-doped graphene is n-type. Ni-doped graphene shows no doping effect, but localized states are found in valence bands.

The Fermi potentials of Ag-doped graphene with different Ag dopant densities are plotted in **Figure 116**. Fermi potential is the energy difference between Fermi level and intrinsic Fermi level and density of Ag dopants is defined by molar fraction = number of Ag atoms / number of C atoms.

Using DFT, Ag-doped graphene and Ni-doped graphene are studied in this work, including their E-k and PDOS. It is found that Ag dopants can dope graphene n-type, while Ni distort the E-k of graphene and does not induce doping. Hence, it is suggested that Ag can be used to dope graphene transparent electrodes in order to increase its conductance. In the further study, more metals will be evaluated as well as varying doping densities.

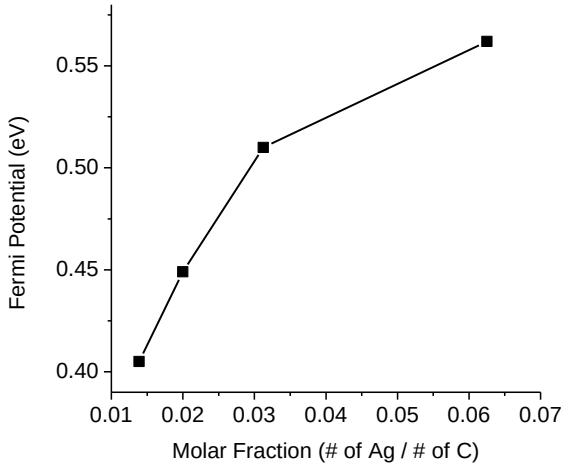


Figure 116: Fermi potential of Ag-doped graphene vs. density of Ag dopants

2. Surface Doping using Metallic Nanoparticles

In this section, the main focus will be the suface doping on molybdenum disulphide (MoS_2), by metallic nanoparticles (NPs) (**Figure 117**).

Since Pt NPs lead to the highest doping on MoS_2 **[11]**and at the same time is stable, the simulation for doped MoS_2 focuses on exploration of Pt NPs in detail. *Ab-initio* density functional theory (DFT) calculations were performed. Since, MoS_2 in general is naturally doped n-type, this n-type doping is simulated by using Cl atoms.

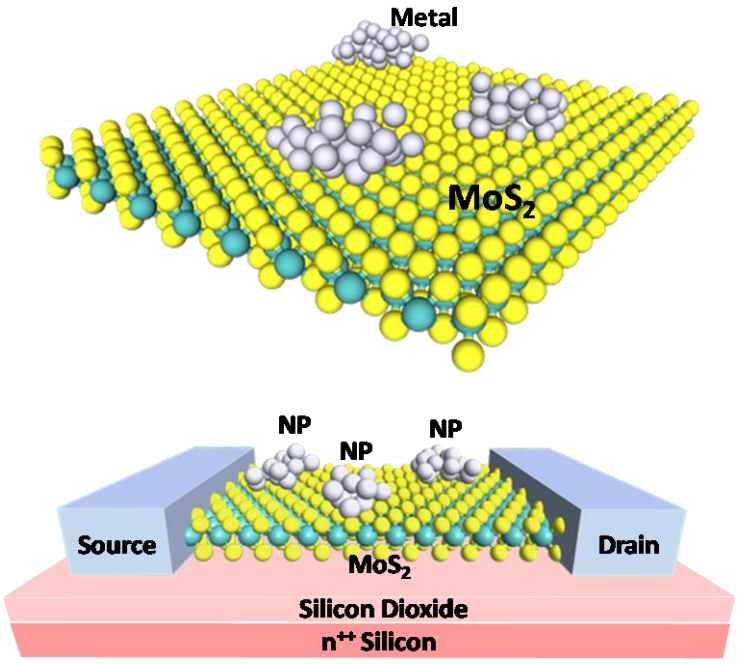


Figure 117: Schematic diagram of a MoS_2 flake doped with metallic nanoparticles. The bottom schematic is a back-gated FET based on NP doped MoS_2.

Since DFT only utilizes periodic boundary conditions with mono-crystalline materials, metal-MoS_2-xClx system is modeled by a unit cell, which is periodic along lattice vector ***a*** and ***b*** and separated by vacuum in the *c* direction, as shown in **Figure 118**. The unit cell contains a doped MoS_2 layer with Cl atoms as dopants, topped by a thin film of Pt to emulate the Pt island. The mean absolute strain is 1.35% due to a slight lattice mismatch. All the atoms are allowed to relax.

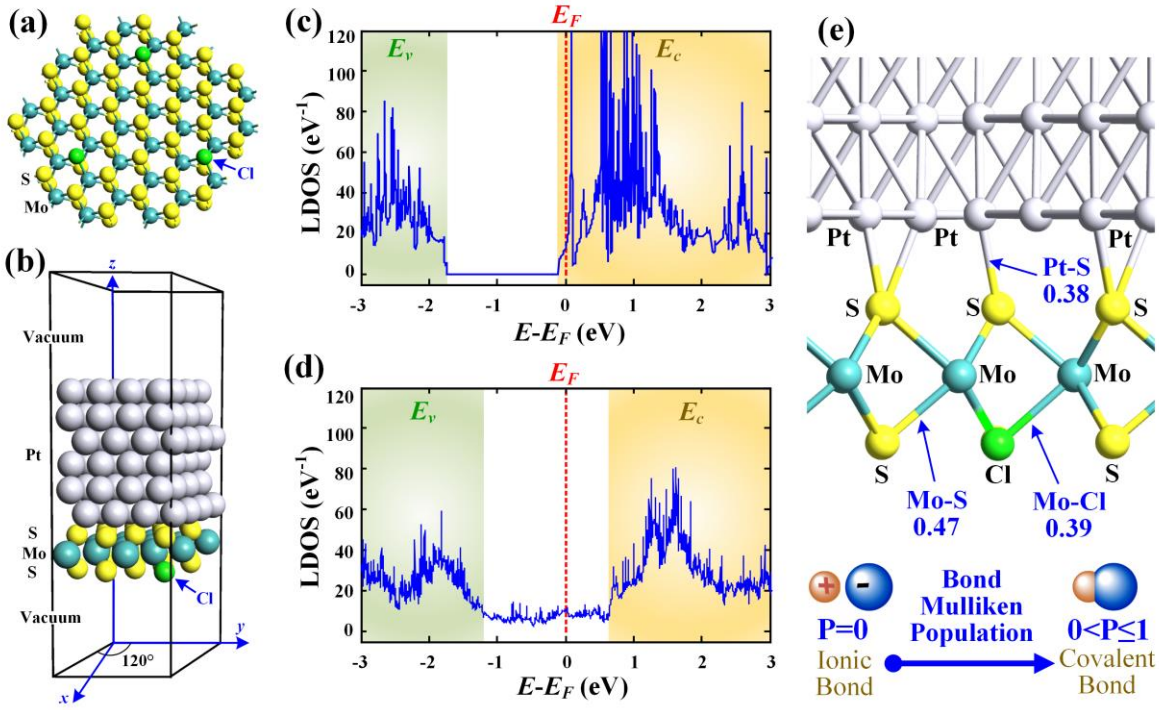


Figure 118. DFT simulation of Pt NP on MoS_2.

(a) The top view of MoS_2 with incorporated Cl atoms in order to simulate the n-type doping in MoS_2. (b) The schematic view of MoS_2-Cl-Pt system. (c) The local density of states diagram of MoS_2-Cl. The orange shaded region denotes the conduction band while the green shaded region denotes the valence band and the white region in between is the bandgap. The Fermi-level, denoted by the red dashed line lies in the conduction band clearly indicating an n-doped MoS_2. (d) After incorporation of Pt, the Fermi-level moves away from the conduction band indicating p-type doping by the Pt. (e) Schematic showing the Mulliken Population (P) for Mo-S bond (0.47), Mo-Cl bond (0.39) and Pt-S bond (0.38). P = 0 denotes ionic bond while P > 0 denote covalent bond. Thus, the positive value of P for Pt-S bond signifies that Pt forms covalent bond with the S of MoS_2.

It is important to note that the study of the metal-2D material interfaces (**Figure 118b**)

requires careful treatment of the van der Waals (vdW) interaction between them. In order to reproduce such nonlocal dispersive force, which are important in weakly bonded systems, DFT-D2 approach **[238]** is used, where a semi-empirical dispersion potential described by a simple pair-wise force field is added to the conventional Kohn-Sham DFT energy.

Local density approximation (LDA) **[230]** is adopted for the exchange correlations, together with with either the double-ζ polarized basis set for expanding electronic density. The calculations are performed using Atomistix ToolKit (ATK) **[242]**. 8×8×1 k-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 200 Rydberg and the maximum force is 0.05 eV/Å for geometry optimizations.

The density of state diagrams before and after the incorporation of Pt NPs are shown in **Figure 118c** and **d** respectively. As is clear from the figures, after the incorporation of Pt NPs the Fermi level (denoted by the dashed line) shifts below the conduction band indicating p-type doping by the Pt NPs. Mulliken population analysis (**Figure 118e**) is also performed to understand the nature of bonding between Pt and MoS_2. Bond Mulliken population (P) represents the electronic charge distribution in a molecule and the nature of the molecular orbitals for a pair of atoms **[328]**. The value of P varies from 0 to 1, where P = 0 and 0 < P <= 1 indicate ionic and covalent bonds, respectively. For covalent bonding, the numerical value of P indicates the strength of the bond. From **Figure 118e** it is clear that Pt forms covalent bonds with the Sulfur of MoS_2 and the value of P for Pt-S bond is found to be 0.38.

To better understand the doping effect of Pt NPs on MoS_2, Raman Spectroscopy is used to analyze the effect of Pt NPs **[11]**. For MoS_2 with NPs, the E^1_{2g} and A_{1g} peaks are shifted towards the right, indicating p-type doping **[329]** (**Figure 119a** inset). This Raman shift can also be supported by DFT simulations (**Figure 119**).

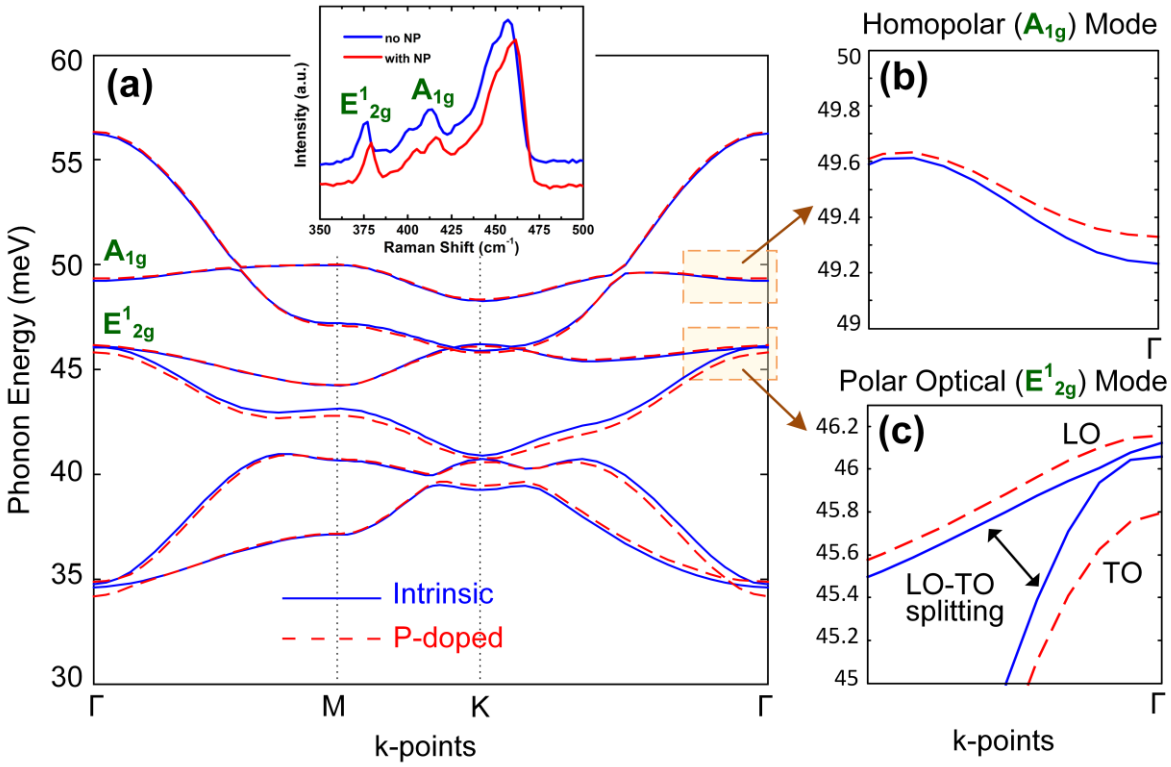


Figure 119. Simulation of phonon spectra of p-doped MoS_2.

(a) Phonon spectra of intrinsic and p-doped MoS_2 (molar fraction 0.1%) calculated by DFT. Inset shows Raman spectra of intrinsic and p-doped MoS_2 measured in experiments. (b,c) Zoom of A_{1g} mode and E^1_{2g} mode at Γ point. In (b), doping increases the phonon energy of homopolar mode (A_{1g}), and hence, the Raman peak corresponding to A_{1g} mode shifts to the right, as shown in inset of (a). In (c), doping increases macroscopic polarization and thus increases LO-TO (longitudinal optical - transverse optical) splitting.

Using this surface doping technique, it is shown that Pt nanoparticles can lead to as large as 137 V shift in threshold voltage of a back gated monolayered MoS_2 FET **[11]**. Moreover the first p-type WSe_2 doped with Pt NPs is demonstrated **[11]**.

3. Surface Doping using XeF_2

It is also shown that by treating some 2D materials using XeF_2 gas, F atoms can be attached to the surfaces, inducing an n-type doping. As shown in the work below (**Figure 120**), XeF_2 treatment on a GaSe back-gate FET can turn a p-type device into n-type. XPS spectra show that there is no shift on the Ga peaks while a shift of the Se peaks can be observed, indicating the formation of surface Se-F bonds.

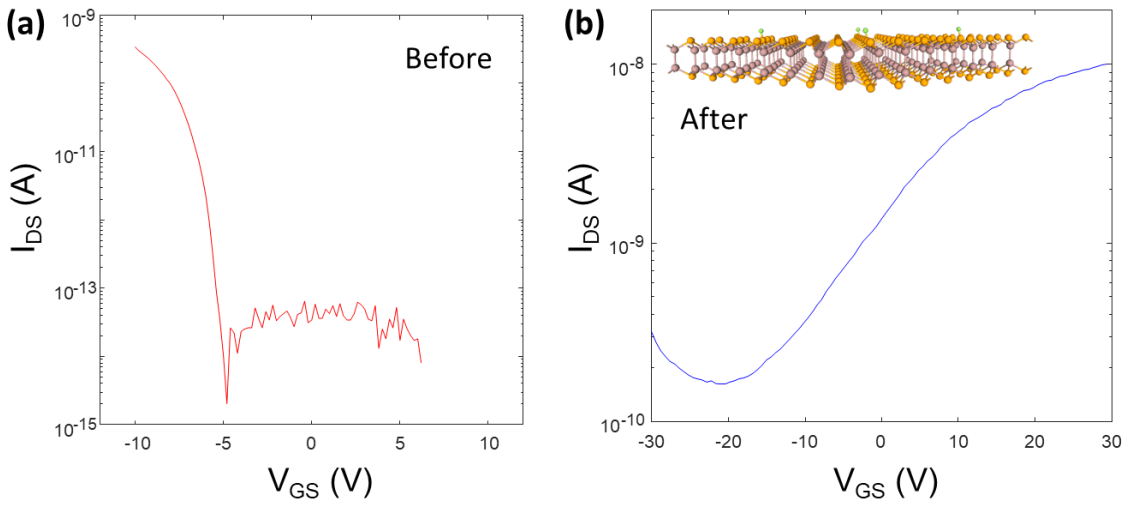


Figure 120: I_{DS}-V_{GS} curves of a GaSe FET before and after XeF_2 treatment.

Note that XeF_2 gas cannot be used to dope MoS2 because XeF_2 can etch MoS_2 with all gas products produced, as discussed in **Chapter II, Section E**.

C. Intercalation Doping of Graphene

1. Doping Graphene for Transparent Electrodes

The electrical and optical properties of FLG can be varied by tuning the number of layers and doping density (**Figure 121**). While increasing the number of layers increases the

available modes for conduction and improves the electrical sheet resistivity, it also reduces the optical transmittance.

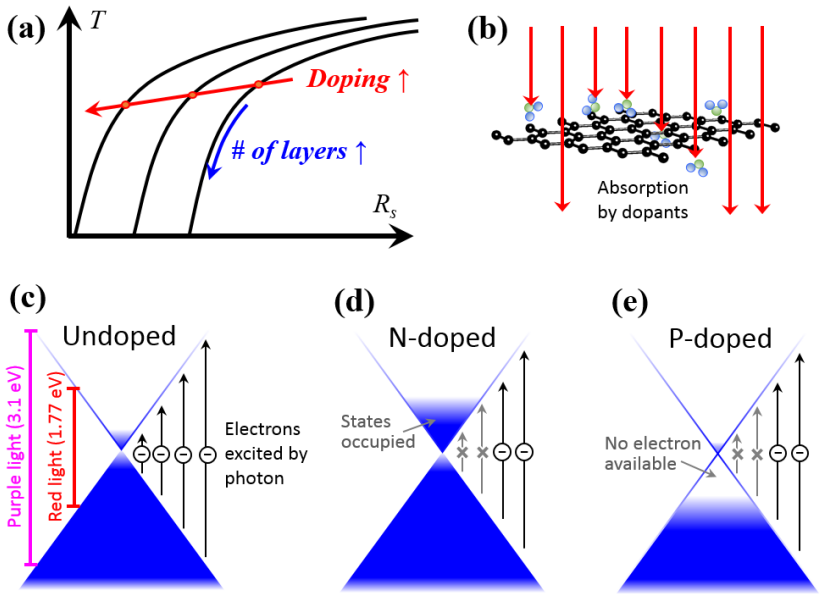


Figure 121. Schmatic showing doping effects on graphene transparency electrodes. (a) Effect of doping and number (#) of layers in terms of transmittance (*T*) and sheet resistance (R_s). (b) Schematic showing optical absorption by dopants. (c) Band diagram showing photoexcited electrons in energy range 0 to +∞ eV, compared with visible light ranging in 1.77 eV to 3.1 eV. (d) N-doped graphene where low energy photons cannot excite eletrons due to occupied conduction band states. (e) P-doped graphene where low energy photons cannot excite eletrons due to absence of electrons in valence band states.

Intrinsic FLG has a very low electron density, which leads to low electrical conductivity. Doping of FLG is an effective way to increase the electron density, and improve the electrical conductivity. However, the dopants act as scattering centers due to Coulomb

potential, and reduce the carrier mobility in graphene. Therefore, the dopant density needs to be tuned for the optimum electrical conductivity. Several methods are being investigated for doping of FLG **[272]** and tuning its work function, which are be discussed below. It is necessary to note that the optical transmittance (*T*) can also be affected by doping. One mechanism is that *T* gets reduced slightly by the dopants added (**Figure 121b**), as observed in experiments **[316]**, **[161]**, **[317]**. The other mechanism, which can increase *T*, is due to the decrease of energy range of photoexcited electrons, as shown in **Figure 121c, d, e**. However, the second mechanism does not take effect till graphene is highly doped (Fermi level moved by at least 1.77 eV /2 = 0.89 eV so that visible light is absorbed less).

2. Doping Graphene for Interconnects and Passives

Graphene, in addition to its planar structure and outstanding electrical properties (such as high current density **[330]**), also has fascinating mechanical and thermal properties, which make them very attractive for next-generation interconnects, through-silicon vias (TSVs) and passives **[61]**.

The commonly used copper interconnect suffers from “size effect” and reliability problems in aggressively scaled sizes. Graphene nanoribbon (GNR) based global interconnects can consume significantly less power than their Cu counterparts **[57], [331]** and have great potential to solve the problems of Cu due to its high electrical conductivity, thermal conductivity, current tolerance and mechanical strength.

However, in a realistic nanoscale graphene interconnect, its conductivity is limited due to additional carrier scatterings, including inter-sheet electron hopping, reduced carrier mean free path from edge scatterings, and bandgap opening for sub-20 nm widths **[142]**. To overcome these challenges, intercalation-doped GNR interconnect was first proposed by Xu et al. **[332]** and theoretically proved to beat the resistivity of Cu **[57]** by appropriate

intercalation doping level.

Similarly, a key challenge of MLG for inductor applications is the high series resistance due to the much higher resistivity compared to bulk metals. A recent effort toward demonstrating graphene based on-chip inductors has been done by us **[17]** by using intrinsic and thin MLGs (tens of nm). Although extraordinary inductance (up to 1650 nH/mm^2) was obtained as expected, however, due to the small body thickness and the high resistivity of intrinsic MLG, the fabricated inductors suffer from high series resistance and thus high loss, or low quality factors (*Q*-factors) of ~3. Hence, new technology and/or techniques are needed for achieving high-performance and energy-efficient on-chip inductors based on graphene.

A solution is to employ a specified technique that induce both (i) reduced resistivity and (ii) interlayer decoupling effect in MLG (which will be discussed in the next chapter). Previous theoretical study has shown that in order to match the performance of metals, *doping* of MLG can reduce the resistivity**[57], [332]**. For such passive applications based on MLG, *intercalation doping*, resulting in graphite intercalation compounds (GICs), is advantageous over other doping techniques, including substitution doping, surface doping, electrostatic doping, etc., in terms of stability, efficiency and preservation of graphene crystal quality**[10]**. Most importantly, intercalation doping can eliminate the interlayer coupling (see the next chapter), and recover the electronic properties (energy dispersion, effective mass, mobility, etc.) of MLG to its few-layer or monolayer form, which makes intercalated MLG based inductors very promising.

Intercalated graphene/MLG, or namely graphite intercalation compounds (GICs) have a long research history, and have shown surprising properties **[333], [334]**. Several candidates as intercalation guests (dopants) have been identified that can improve the conductivity of

MLG, such as alkali metals, halogens (Cl_2, Br_2, ICl, etc.), and halides (AsF_5, $AuCl_3$, $FeCl_3$, etc.) **[12], [15], [323], [333]–[340]**.

3. Intercalation Doping using Bromine

Among many intercalation doping options, Br intercalation is interesting due to its simple process and high efficiency. As shown in **Figure 122**, Br_2 molecules can diffuse into in the gaps between graphene layers forming intercalate layers and remain stable, which induce bands with high density of states below the Dirac point (and intrinsic Fermi level E_{Fi}) of the graphene layers. These impurity states attract electrons from graphene, generating hole carriers in the valence band of graphene resulting in p-type doping (**Figure 123**).

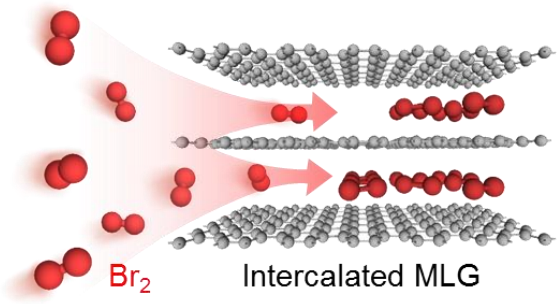


Figure 122: Illustration of bromine intercalation.

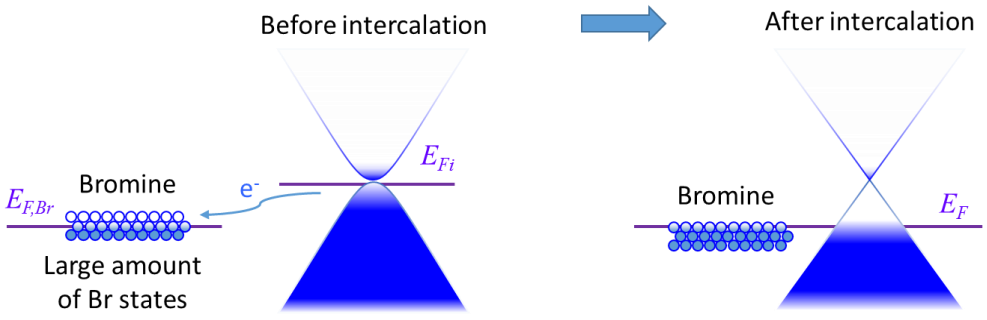


Figure 123: Illustration of the effect of bromine intercalation on band structures.

Since DFT only utilizes periodic boundary conditions with mono-crystalline materials, graphite intercalation compound (GIC) systems (**Figure 124A**) are modeled by a unit cell, which is periodic along all the three lattice vectors (**Figure 124B**). The unit cell contains intrinsic graphene layers intercalated by Br_2 layer(s). Br_2 molecules are aligned in the solid Br crystal form **[333]**. All the atoms as well as the lattice parameters are allowed to relax.

It is important to note that the study of the Br_2-graphene interface requires careful treatment of the van der Waals (vdW) interaction between them, which is usually missing in previous studies of graphite intercalation compound **[339]**. In order to reproduce such nonlocal dispersive force, which are important in weakly bonded systems, DFT-D2 approach **[238]** is used, where a semi-empirical dispersion potential described by a simple pair-wise force field is added to the conventional Kohn-Sham DFT energy.

Perdew-Burke-Ernzerh variant of Generalized Gradient Approximation (GGA) **[228]** is adopted for the exchange correlations, together with Hartwigsen-Goedecker-Hutter (HGH) basis set for expanding electronic density. The calculations are performed using Atomistix ToolKit (ATK) **[242]**. 9×5×5 *k*-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 200 Rydberg and the maximum force is 0.05 eV/Å for geometry optimizations.

The red curves in **Figure 125** show the energy states of Br intercalation guest, which are below the Dirac point (or intrinsic Fermi level) of the graphene layers. Hence, these impurity states attract electrons from the graphene layers, generating holes in the valence band of the graphene layers and pull down the Fermi level to the bromine levels and thus into the valence band (or p-type doped). The process is illustrated in **Figure 123** below.

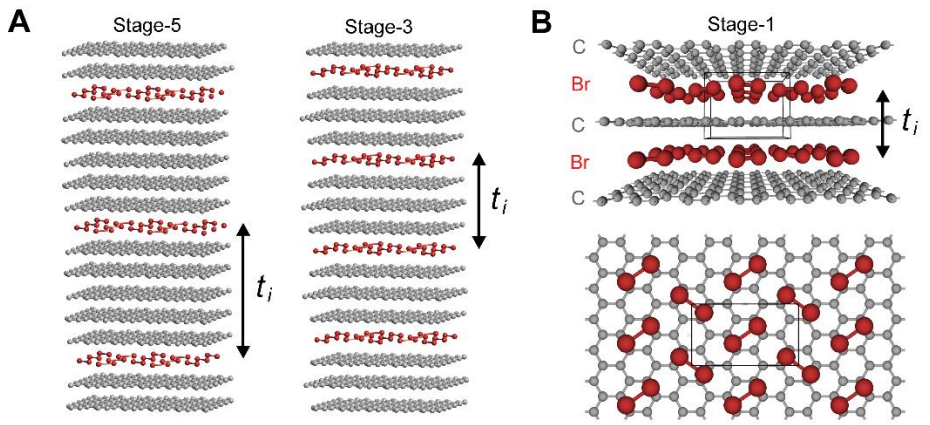


Figure 124: Schematic of Br-intercalated MLG.

(A) Schematic of stage-5 and stage-3 Br-intercalated MLG (GIC). Stage # = ratio of graphene layer # over intercalation layer #. (B) Side view and top view of Br-intercalated MLG (stage-1). The black cuboid/rectangle represents the unit cell. t_i represents the vertical periodicity (distance between two adjacent intercalation dopant layers).

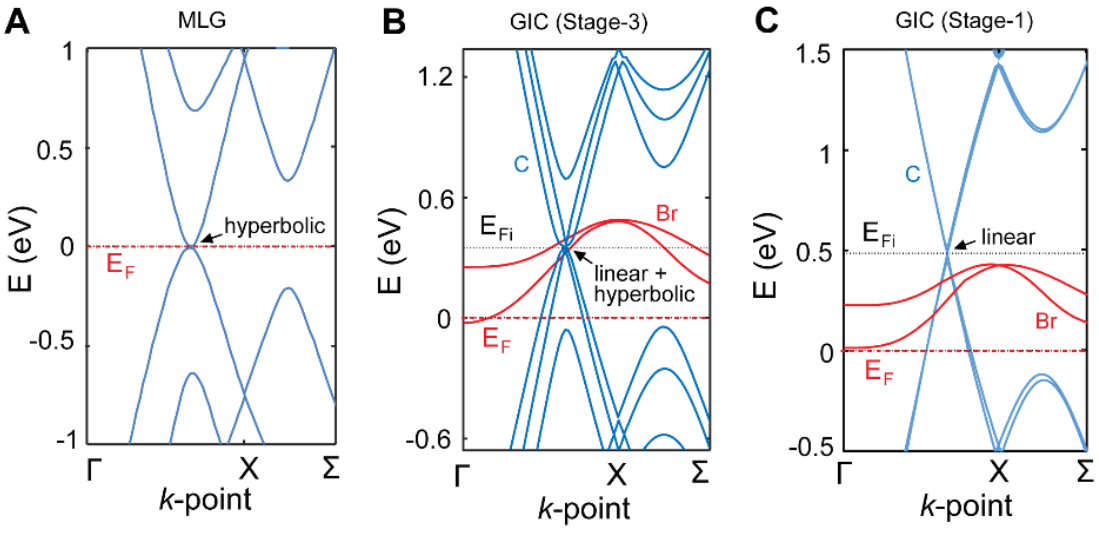


Figure 125: Band structures of Br-intercalated MLG.

(A) Intrinsic MLG, (B) stage-3 and (C) stage-1 Br intercalated MLG.

In the next chapter, the first demonstration of on-chip inductors based on intercalated-graphene will be presented, using the bromine as intercalation guest. By using Br-intercalated multilayer graphene into on-chip inductors, one can harvest 1.5-fold higher inductance density with undiminished performance (Q-factors up to 12).

4. Intercalation Doping using $FeCl_3$

$FeCl_3$ is a crystal with high density of localized states near the Fermi level, which can adopt large amount of electrons from the materials next to it, as shown by DFT simulation in **Figure 126**.

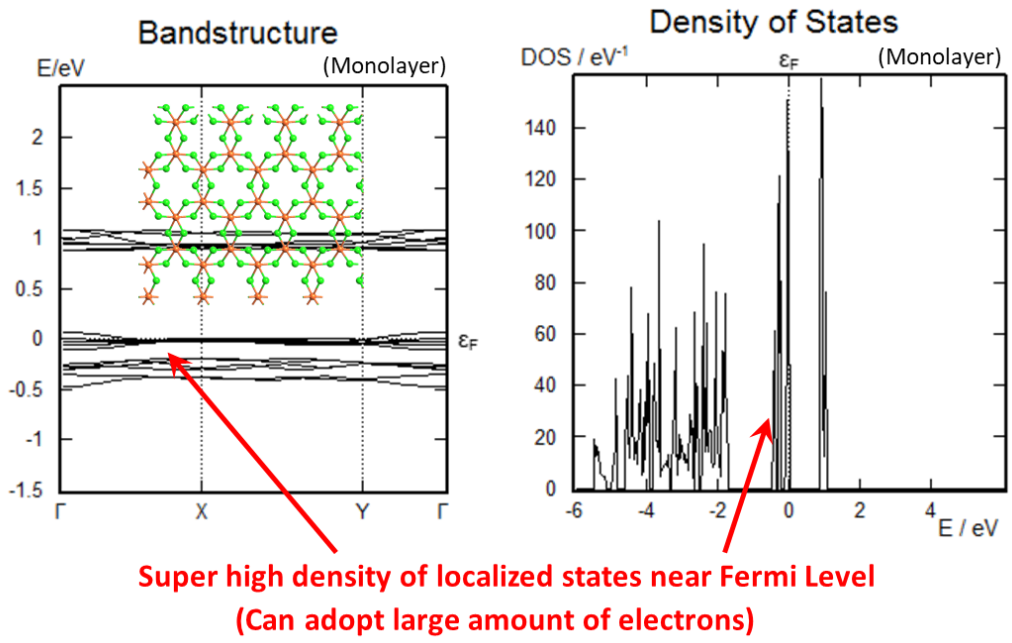


Figure 126: Material properties of $FeCl_3$.

It is important to note that the study of the $FeCl_3$-graphene interface requires careful

treatment of the van der Waals (vdW) interaction between them, which is usually missing in previous studies of graphite intercalation compound **[339]**. In order to reproduce such nonlocal dispersive force, which are important in weakly bonded systems, DFT-D2 approach **[236]–[238]** is used, where a semi-empirical dispersion potential described by a simple pair-wise force field is added to the conventional Kohn-Sham DFT energy. Perdew-Burke-Ernzerh variant of Generalized Gradient Approximation (GGA) **[229]** is adopted for the exchange correlations, together with Hartwigsen-Goedecker-Hutter (HGH) basis set for expanding electronic density. The calculations are performed using Atomistix ToolKit (ATK) **[242]**. 4×4×4 *k*-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 200 Rydberg and the maximum force is 0.05 eV/Å for geometry optimizations.

The structures of $FeCl_3$ intercalation doped graphene are shown in **Figure 127a,b**. DFT calculations are employed to understand the intercalation doping effect. The calculated band structures of $FeCl_3$ intercalation doped bilayer, trilayer, and 4-layer graphene are shown in **Figure 127c,d,e**. Their Dirac points are above the Femi level indicating a p-type doping. The light orange zones in **Figure 127c,d,e** show the states of $FeCl_3$, which absorb the electrons from graphene. The band structure of intercalation doped bilayer, trilayer, and 4-layer graphene have linear dispersion near the Dirac point, implying that the Bernal stacking order is broken by $FeCl_3$. The shift of Fermi level increases from ~0.55 eV (bilayer) to ~0.7 eV (4-layers), which matches the conductivity trend obtained via experimental measurement.

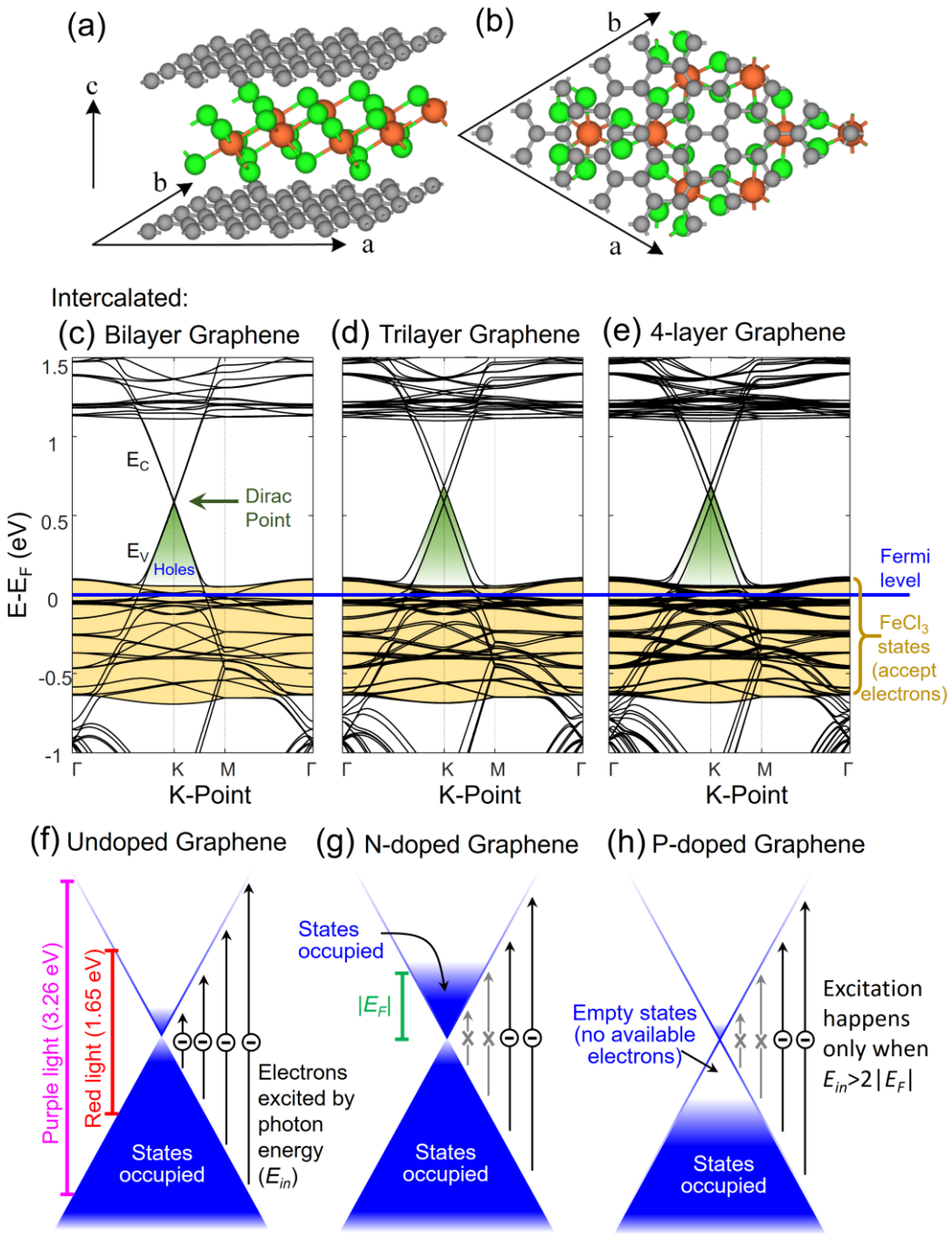


Figure 127. Simulation of $FeCl_3$ doped graphene.

Schematic illustration of side view (a) and top view (b) of $FeCl_3$ intercalation doped bilayer graphene. Band structure of intercalated bilayer (c), trilayer graphene (d), and 4-layer graphene (e). Schematic band diagrams illustrating the absorption of photons due to interband interactions in undoped (f), n-doped (g) and p-doped (h) graphene.

It is worth noting that the p-type doping is very suitable for the applications which expose graphene to moisture because graphene is usually p-type due to the doping effect from the environment. On the other hand, the absorption of photon by graphene due to interband interactions will only be prohibited when the incident photon energy E_{in} is smaller than $2|E_F|$ (Pauli blocking). For visible light spectrum (E_{in} = 1.65-3.26 eV), there is no possibility of Pauli blocking for reasonable graphene doping level ($|E_F| \sim 0.55 - 0.7$ eV, $2|E_F| < E_{in}$). **Figure 127f-h** illustrate this phenomenon. Hence, the transmittance in the visible light range almost remains the same after doping, which has also been shown by transmittance measurements in **[161]**.

The comparison of sheet resistance and transmittance of our doped CVD graphene with doped exfoliated/CVD graphene reported by others **[161]**, **[341]**, **[342]**, ITO **[343]**, CNT mesh **[344]**, Ag mesh **[343]**, reduced graphene **[345]**, and other undoped CVD graphene**[158]**, are shown in **Figure 128**. It can be observed that our 4-layer doped CVD graphene exhibits the best combination of sheet resistance (20 Ω/□) and transmittance (~ 90%) among all previously reported transparent conductors. From the data, it can also be observed that although ITO film can attain the smallest sheet resistance, which is even smaller than the sheet resistance of theoretical calculated value of undoped monolayer graphene (red pentagon) **[161]**, the thickness of ITO should be above 100 nm, which is much larger than 3-4 layer graphene (2 nm) and hence the transmittance is much lower (~70%). Similarly, the transmittance of Ag mesh significantly decreases to ~80% when its sheet resistance is around 10 Ω/□ **[161]**. It is also difficult to maintain the balance of small sheet resistance and large transmittance on CNT mesh. Hence, doped graphene seems most suitable for high performance transparent conductor applications.

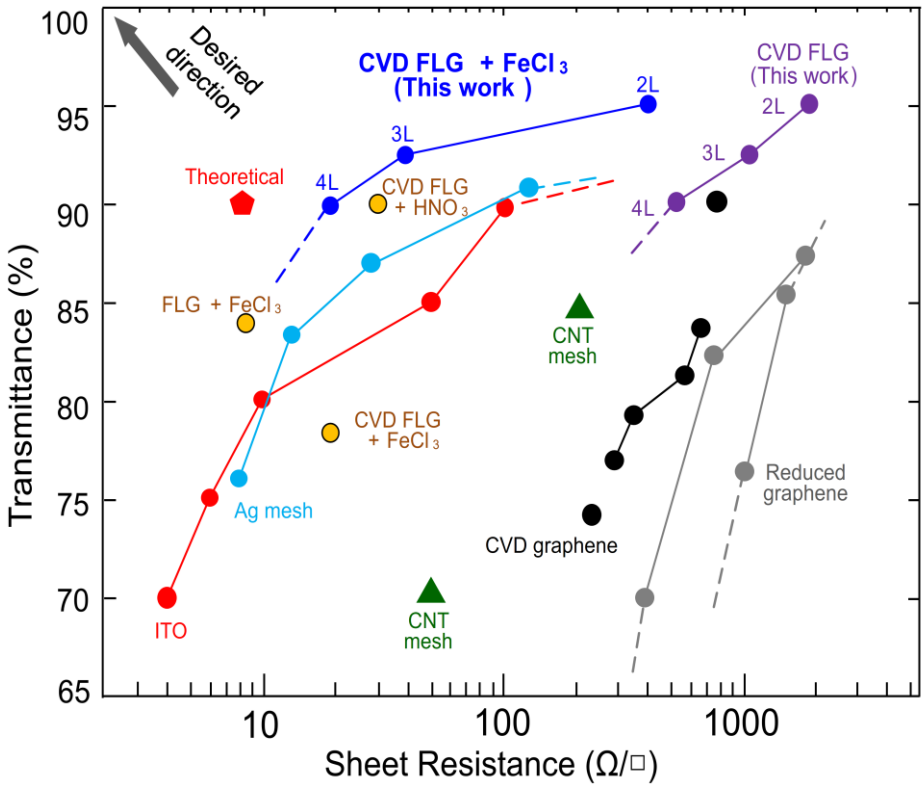


Figure 128: Sheet resistance/transmittance of $FeCl_3$ doped graphene.

Comparison of sheet resistance/transmittance of our graphene sample with other transparent electrodes reported in literature. Note that the electrical measurement was done on SiO_2/Si substrate, while the transmittance was measured on transparent (quartz) substrate. However, the CVD FLG samples were synthesized and doped under the same condition.

D. Intercalation Doping of MoS_2 by $FeCl_3$

1. Introduction

The intercalation of multilayer graphene or graphite using $FeCl_3$ has been well studied for the past decades **[133]**. However, the application of the same technique has not been

shown in TMD materials such as MoS_2. In this section, the first study of intercalation doping of MoS_2 using $FeCl_3$ is presented. Similar to the case of graphene, DFT simulation shows that a p-type doping can be achieved in MoS_2 as well. Subsequently, intercalated multilayer MoS_2 is demonstrated experimentally, the transistor of which shows a clear p-type turn-on behavior. Finally, as a prototype of application, a complementary logic gate – an inverter is demonstrated based on natural n-type MoS_2 and intercalated p-type MoS_2.

2. Simulation

DFT calculations are employed to understand the intercalation doping effect. The methodology is kept the same as that in the previous section. As the first attempt, intercalation for bilayer MoS_2 is studied (**Figure 129**).

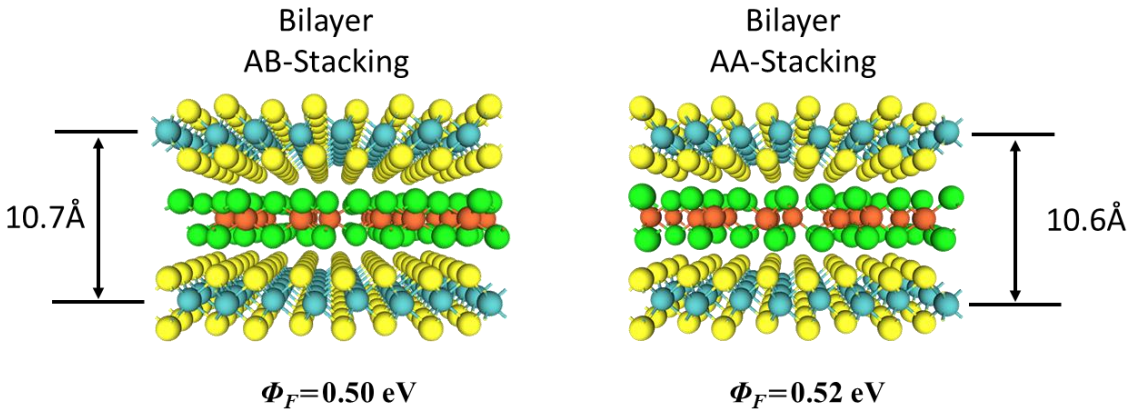


Figure 129: Optimized atomic structures of intercalated bilayer MoS_2.

Two types of stacking orders, AB-stacking and AA-stacking are shown, both of which show very similar properties.

The electron density profile and band structure of $FeCl_3$ intercalated 2L-MoS_2 was calculated (**Figure 130**). The simulation show that $FeCl_3$ intercalation doping introduces p-

type doping ($|E_F|$ ~ 0.5 eV doping level) in bilayer MoS_2 because of charge transfer between $FeCl_3$ acceptor states and MoS_2.

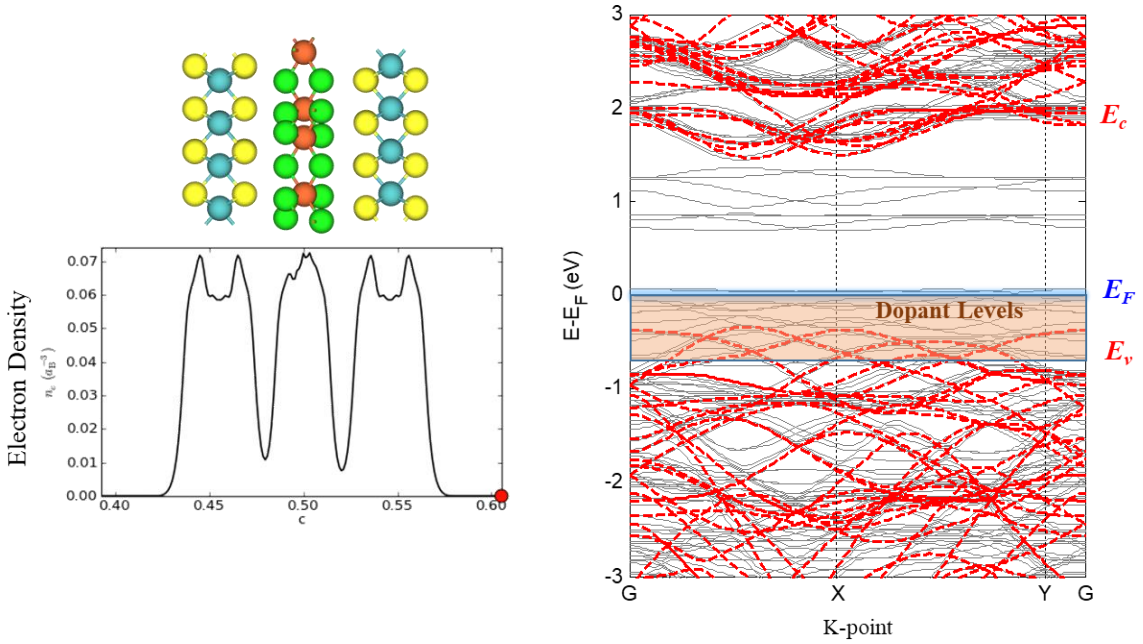


Figure 130: Electron density profile and band structure of intercalated 2L-MoS_2. Left: valence electron density at different positions along c-axis (perpendicular to the 2D plane). Right: band structure.

The simulations are further extended to tri-layer and bulk MoS_2 as well, the schematics and band structures of which are shown in **Figure 131** and **Figure 132**. As shown in these results, $FeCl_3$ intercalation can also dope multilayer MoS_2 to p-type.

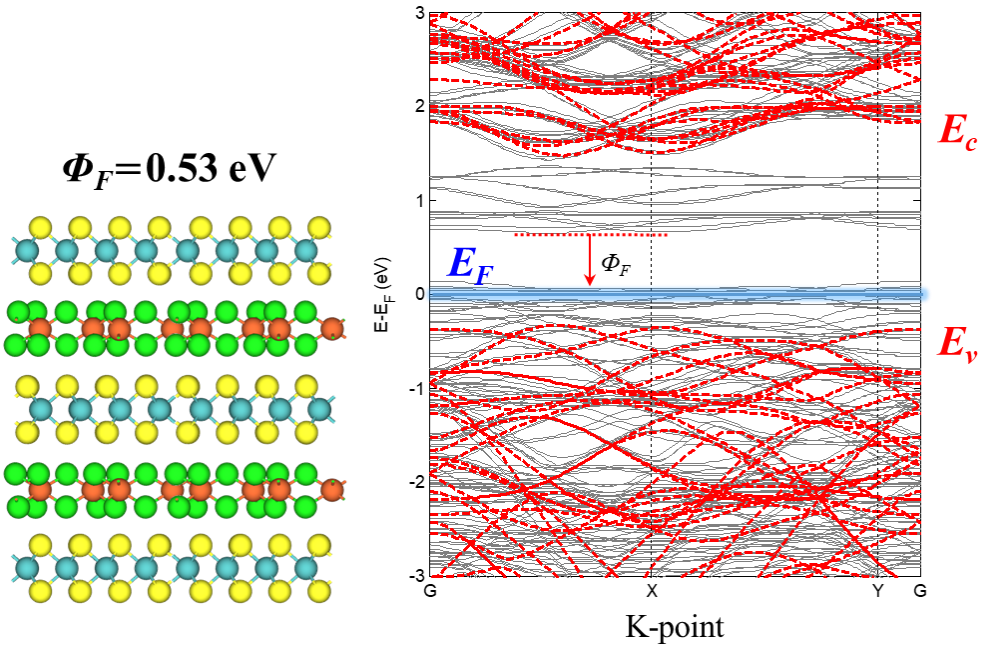


Figure 131: Relaxed structure and band structure of intercalated 3L-MoS_2.

The partial density of states (PDOS) in the MoS_2 layers, for the cases of 1L and bulk, are plotted in **Figure 133**. Similarly, in both cases, a Fermi level shift from the intrinsic Fermi level towards the valence band can be observed, indicating a p-type doping.

3. Preparation of MoS_2 Ribbons

In order to achieve full doping, the MoS_2 flake sizes should be small so that the diffusion distance required for $FeCl_3$ dopants is short. Hence, it is necessary to pattern MoS_2 flakes into ribbons. For such purpose, a relatively simple and clean method – XeF_2 dry etching **[186]** is employed.

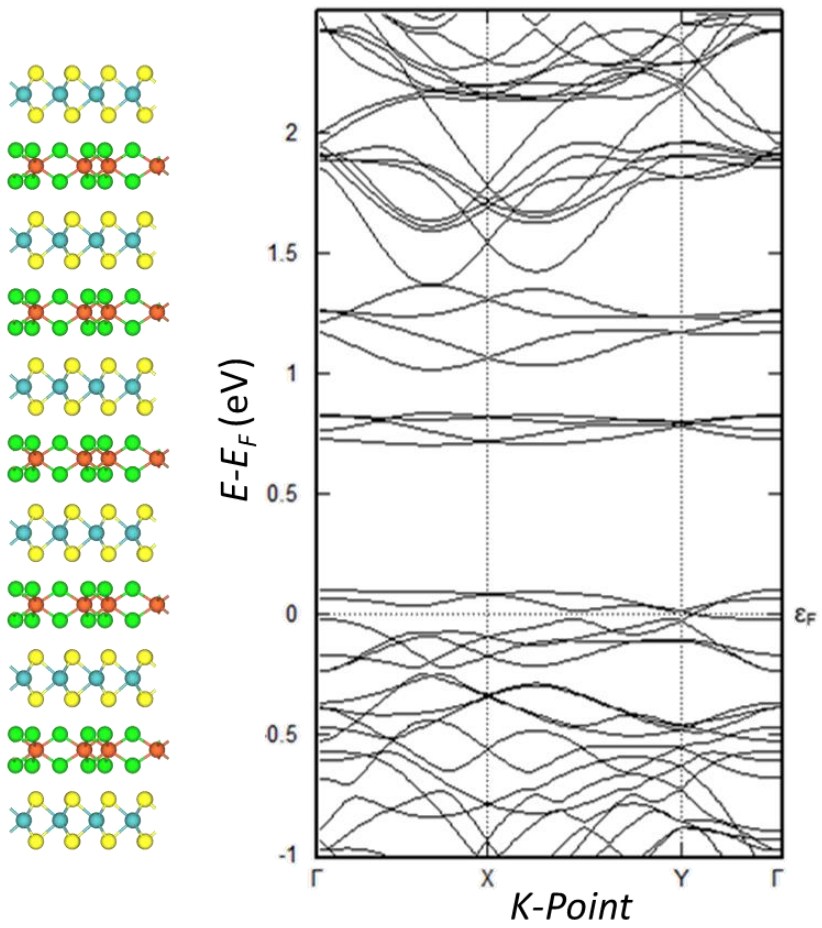


Figure 132: Relaxed structure and band structure of intercalated bulk MoS_2.

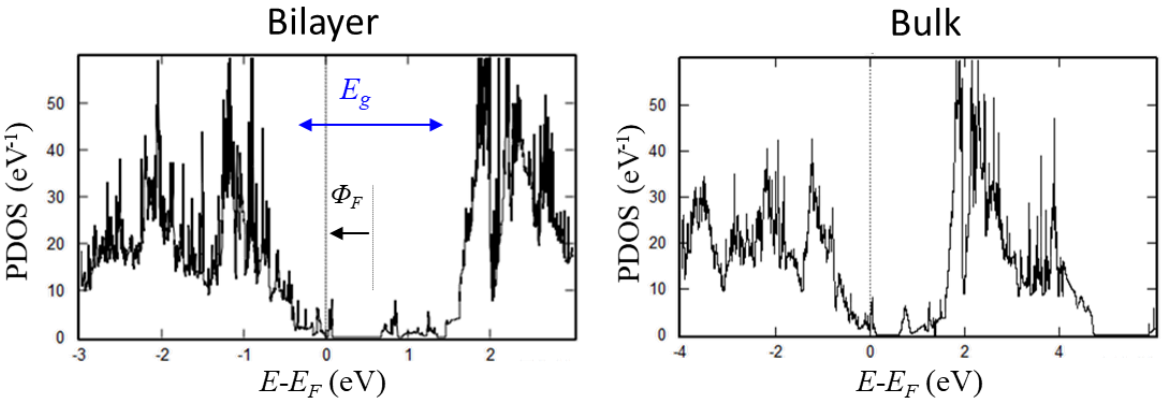


Figure 133: Partial density of states of intercalated 2L and bulk MoS_2.

For developing the process, two different masks for defining the patterns were attempted, including metal Ni and photoresist PMMA (**Figure 134** and **Figure 135**). As shown in **Figure 134**, Ni mask is not robust against over-etching of the isotropic XeF_2 gas phase process, where the narrow ribbons are etched away. While by using PMMA as mask, the both wide and narrow ribbons are patterned (**Figure 135**). A possible reason for this difference between **Figure 134** and **Figure 135** could be that the PMMA gets melted by the heat during etching process and covers the as etched ribbons, thus protecting them from over-etching, as illustrated in **Figure 136**.

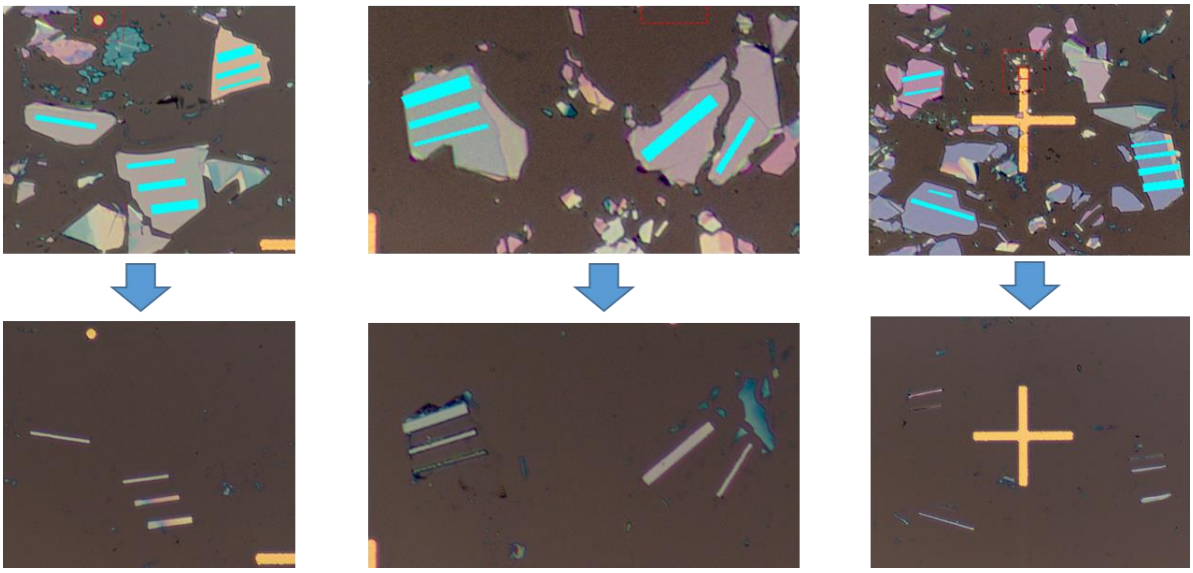


Figure 134: Photos of the XeF_2 dry etching process using Ni as masks.

Top photos: natural MoS_2 flakes before etching. The blue regions are to be covered by Ni while other regions are exposed to XeF_2. Bottom photos: the MoS_2 ribbons after etching.

Hence, the PMMA based method is used to prepare MoS_2 ribbons. After patterning of MoS_2, Pd/Au is deposited and patterned as metal contacts. The reasons for using Pd as the

buffer layer is that first, the Fermi level of Pd will be pinned to the middle of the MoS_2 bandgap and hence both n-type and p-type contacts can be realized; second, Pd is relatively stable and has resistance against corrosive $FeCl_3$ process.

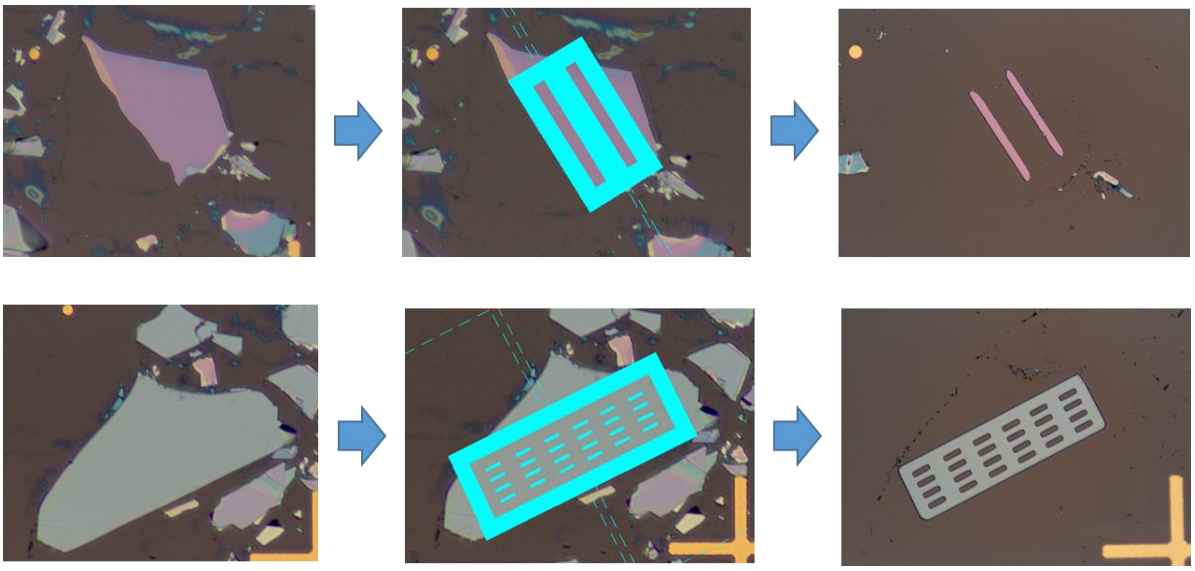


Figure 135: Photos of the dry etching process using PMMA as masks.

Left: natural MoS_2 flakes before etching. Middle: the blue regions are covered by PMMA while other regions are exposed to XeF_2. Right: the MoS_2 ribbons after etching.

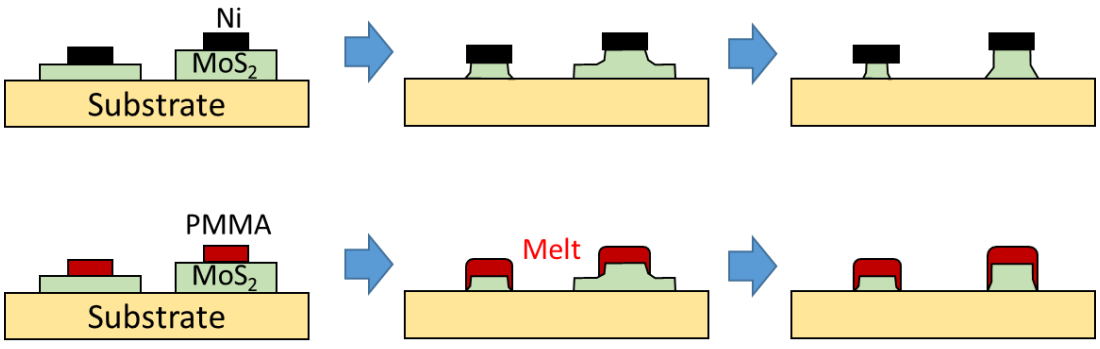


Figure 136: Schematics showing the possible mechanisms of Ni and PMMA masks.

4. Doping Process

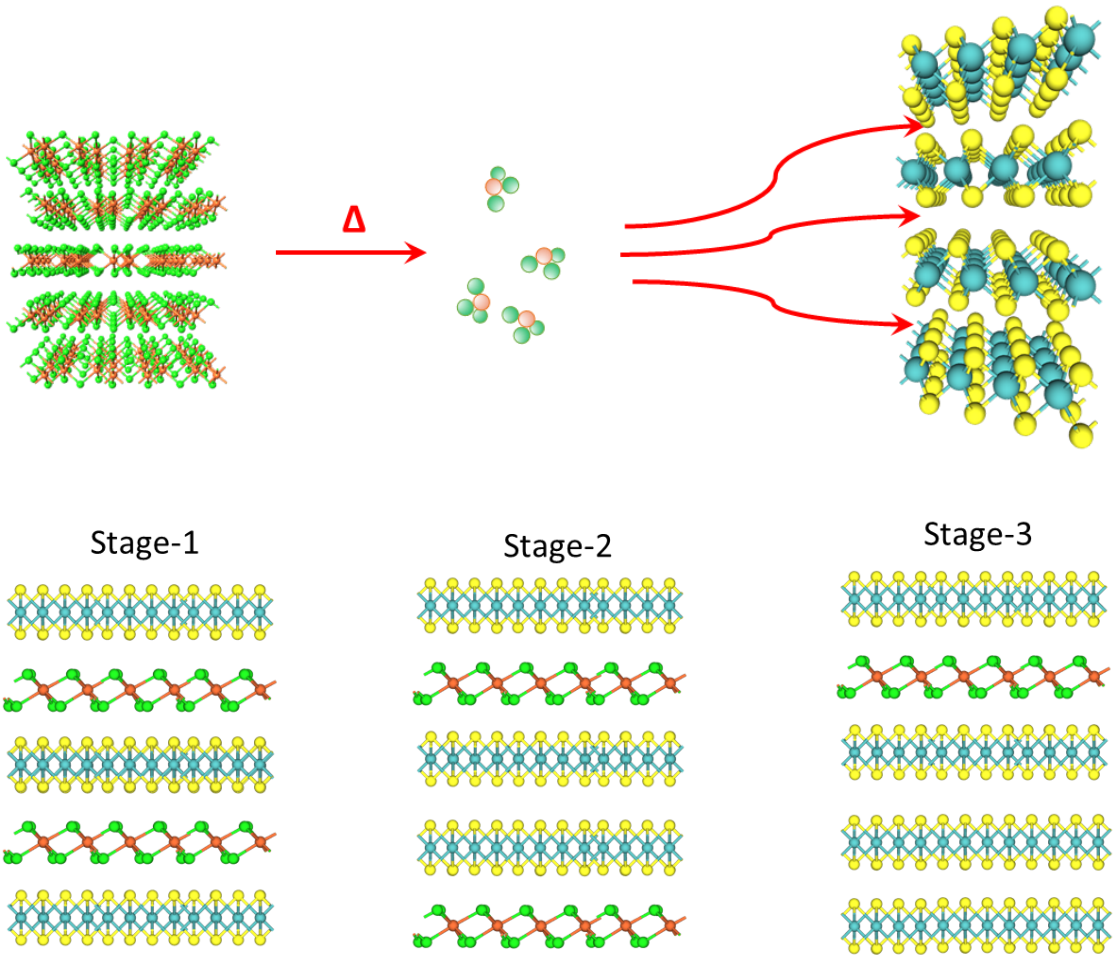


Figure 137: Schematic of intercalation doping process for MoS_2.

$FeCl_3$ (left) is heated up and evaporated into gas phase (middle), and then $FeCl_3$ gas diffuses into the gaps of MoS_2 (right). The bottom figures show schematics of $FeCl_3$ intercalated MoS_2 with different intercalation stages.

The $FeCl_3$ intercalation doping process for MoS_2 ribbons is performed using the similar physical vapor transport method for graphene **[161], [341], [342]** as illustrated in **Figure 137**. After MoS_2 sample is put in a glass tube (**Figure 138**) together with $FeCl_3$ powder, the

pressure in the tube is decreased to ~10^{-1} Torr in a few minutes to remove moisture. Next, He carrier gas transports $FeCl_3$ vapor to MoS_2. The pressure is maintained slightly above 1 atm. The temperature is maintained at 360 °C. $FeCl_3$ evaporates and diffuses in between the MoS_2 layers under high temperature and pressure, and acts as acceptors that increases hole concentration. After 7 hours, the heater is switched off and cooled down to room temperature with high purity He flow.

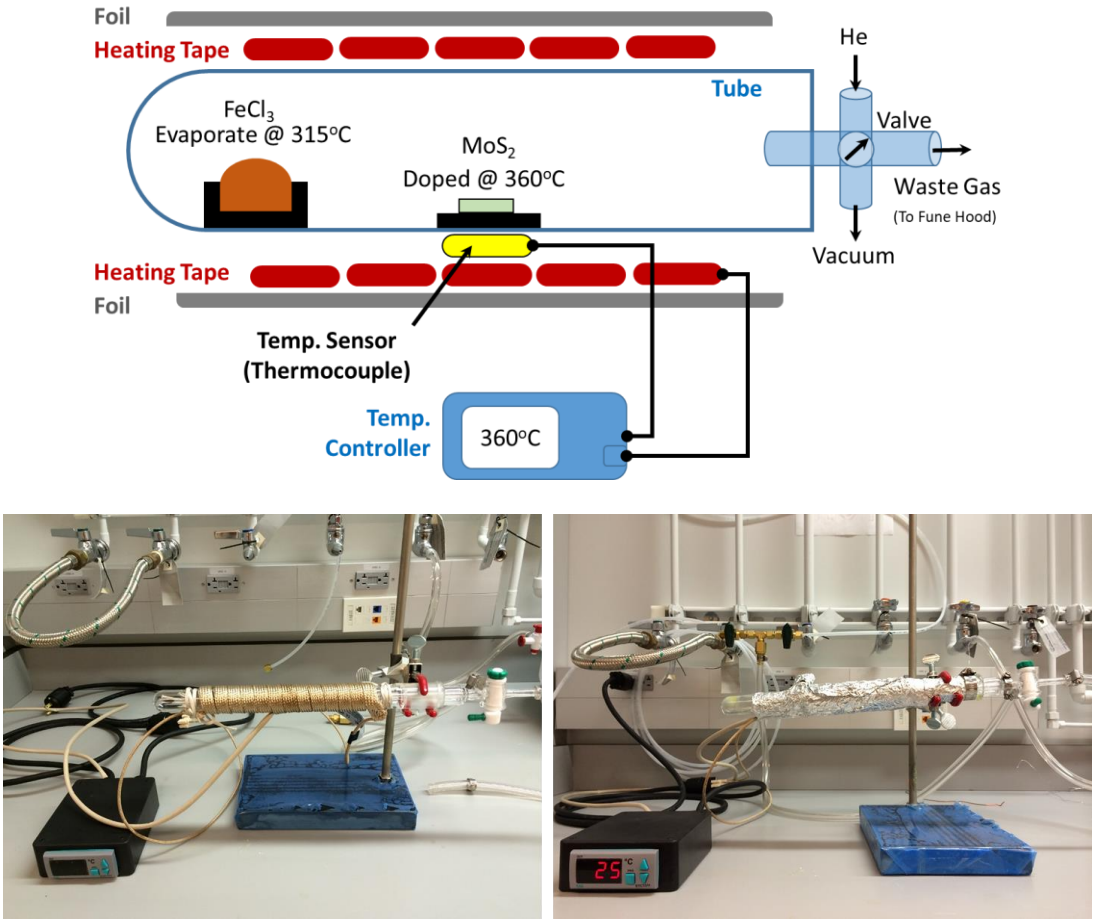


Figure 138: The Experimental setup for intercalation doping.

Top: Schematic of the system; bottom: photos of the system before (left) and after (right) Al foil wrapping.

5. Device Characterization

As shown in **Figure 139**, all the samples turned from natural n-type devices to strong p-type devices. A reduction in the drive current can be observed which can be induced by several reasons:

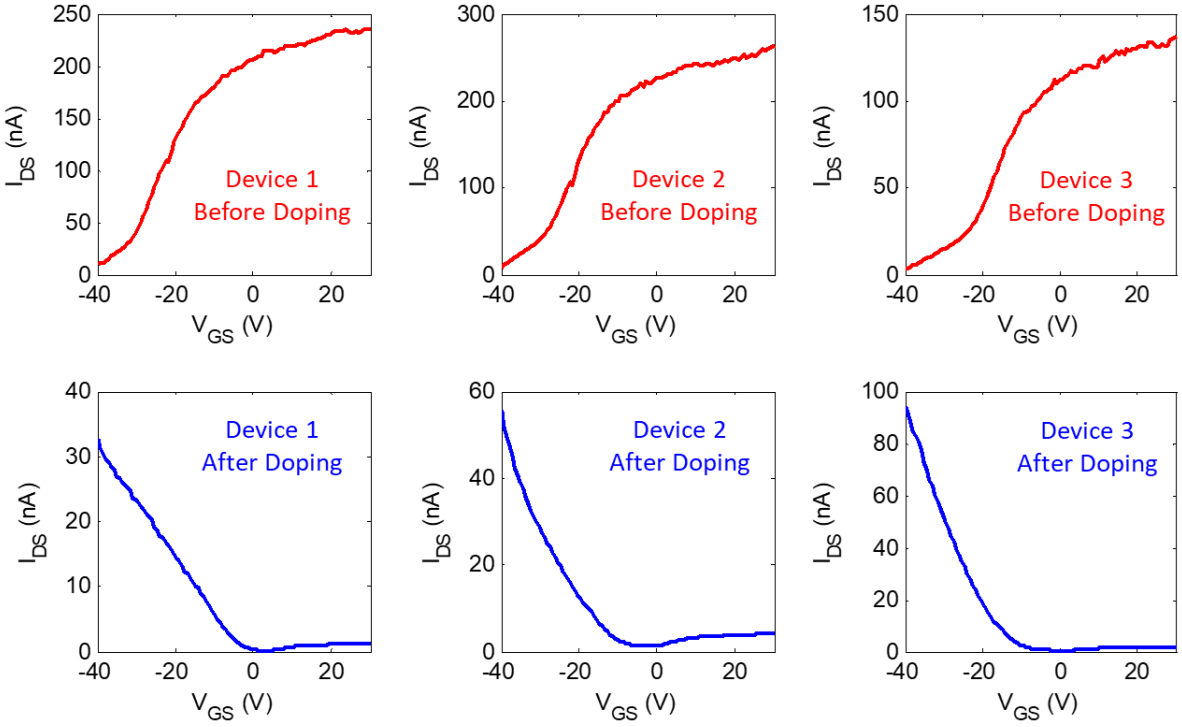


Figure 139: I_{DS}-V_{GS} curves of MoS_2 devices before and after doping.

The devices are back-gated based on multi-layer natural MoS_2 with 90 nm SiO_2 as dielectric. The contacts are Pd/Au (20nm/80nm). 7-hour $FeCl_3$ doping @ 360 C was applied.

First, the hole mobility of MoS_2 is lower than that of electrons;

Second, a degradation in the mobility may happen due to impurity and coulomb scatterings from $FeCl_3$;

Third, an increase of the contact resistance can be expected due to corrosion of contact interfaces.

On the other hand, due to the increase of imperfection in the material, the OFF current at high V_{GS} is very high, thus resulting low ON-OFF ratio.

6. Demonstration of Complementary Inverter

Since p-type MoS_2 devices have been demonstrated, in the last, a complementary logic gate, an inverter consist of an n-type transistor and a p-type transistor is demonstrated. The fabrication process is illustrated in **Figure 140a**. Two adjacent back-gated MoS_2 transistors were first fabricated (**Figure 140b**), and then covered by Al_2O_3 using atomic layer deposition as a protection layer. Afterward, an opening was etched by KOH solution to expose one of the transistors, followed by $FeCl_3$ intercalation (**Figure 140c**).

The voltage transfer curves (VTC, output voltage V_{out} vs. input voltage V_{in}) of the inverter are shown in **Figure 141**. It can be seen that the circuit does show a VTC of inverter. However, the V_{OH} (maximum output voltage) is much smaller than supply voltage V_{DD}, indicating the pull-up network (p-type device) is not strong enough to pull up the output, which is true according to the previous characterization of individual p-type devices.

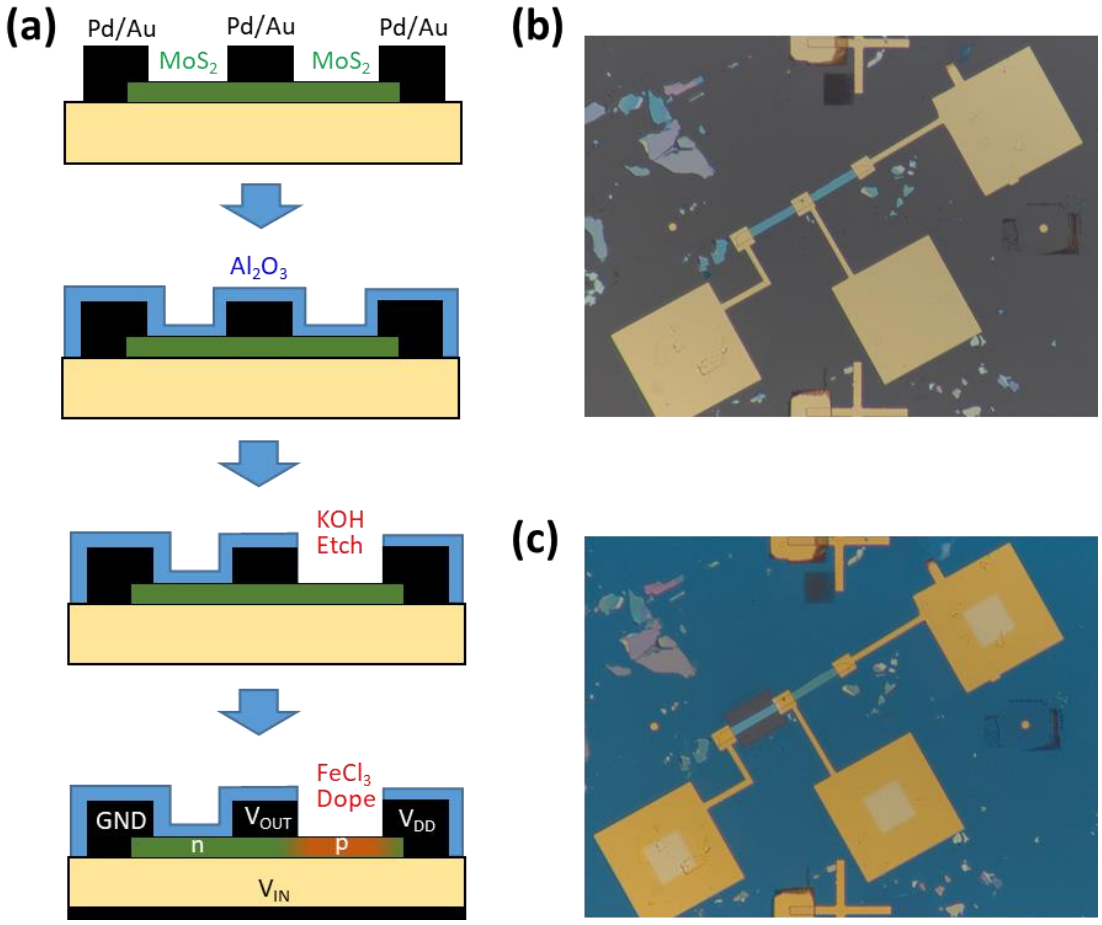


Figure 140: A ML-MoS_2 Inverter.

(a) Fabrication flow; (b) photo before deposition of Al_2O_3; (c) final photo.

Nevertheless, as a first attempt, a demonstration of complementary logic is achieved and there is much space to improve as future works.

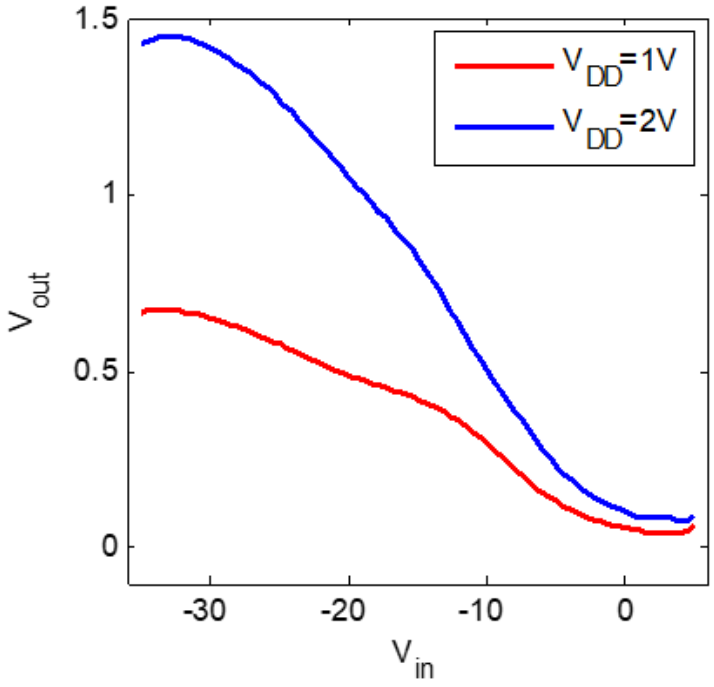


Figure 141: Voltage transfer curves of the MoS_2 inverter.

E. Surface Functionalization by Lewis Acid–Base Chemistry

1. Introduction

Modification of surface electronic states of two-dimensional (2D) atomic layers, via chemical functionalization could significantly enhance their potential for applications. In contrast to bond-breaking and covalent functionalization schemes, it is show that atomic layers with Lewis base character can be selectively surface modified by reacting with Lewis acids, without destroying their original 2D lattice structure and topology. Atomic layers of n-type Indium Selenide (InSe), which has Lewis-base character with population of excess lone pairs of electrons, are converted into planar p-type $[Ti^{4+}{}_n(InSe)]$ complex layers via reaction with Lewis acids, showing an effective and non-destructive strategy for local electronic state modification of solid atomic layers. **[13]** This topo-chemical modification

approach is also shown feasible for other 2D materials such as MoS_2. The Lewis base-acid conjugation can further be used as bridges to connect molecular constructs to form various functional 2D atomic layer hybrid structures with a wide range of chemical characteristics.

InSe features this Lewis base character shared by many other 2D materials. Each InSe layer is composed of a Se-In-In-Se structure, and a van der Waals gap exists between two neighboring Se layers as shown in **Figure 142a**. Under the molecular orbital approximation, each selenium atom has a tetrahedral orbital configuration due to sp^3 hybridization**.** Out of the four sp^3 orbitals, three of them form In-Se bonds, and the remaining one is fully occupied by lone pair electrons. According to Pauli exclusion principle, the fully occupied orbital cannot accept additional electrons to form chemical bond, and this results in the inert nature of most 2D materials. But Lewis-acids featured by empty electron orbitals can accept these lone pair electrons and form stable coordinate covalent bonds. Typical Lewis acids contain metallic ions (e.g.Ti^{4+}, Sn^{4+}, etc.) or boron compounds (such as BCl_3, BH_3, etc.). The reaction between Ti^{4+} (Lewis acid) and InSe (Lewis base) is demonstrated as an example here. InSe samples is immersed into a 0.5 mol/L $TiCl_4$ ethanol solution to react with Ti^{4+}. The lone pair electrons of selenium enter the empty orbitals of Ti^{4+} and form a InSe-Ti coordination complex with the form of $[Ti^{4+}{}_n(InSe)]\cdot Cl^-{}_{4n}$ **[13]**. It is worth to note that only the very superficial layer of Se atoms can react with Ti^{4+}, and only one layer of Ti^{4+} can be anchored by the Se atoms by coordinate bonds. After the InSe surface is fully covered by the Ti^{4+}, the reaction stops and no more Ti^{4+} accumulate on the InSe surface, since there is no more anchor point. Here, ethanol serves as a protic solvent to ionize $TiCl_4$ into Ti^{4+}, so that Ti^{4+} can directly touch the InSe surface and react with it. In a non-protic solvent, the steric hindrance of the Cl^- in tetrahedron $TiCl_4$ molecule prevents the Ti^{4+} from physically contacting the flat InSe surface, as a result non-protic solvents cannot be applied for InSe-Ti

complex synthesis.

2. DFT Simulation

Ab-initio density functional theory (DFT) calculations were performed to verify the Ti^{4+} configuration on InSe surface. The InSe-Ti system is modeled by a unit cell, which is periodic along lattice vector ***a*** and ***b*** and separated by vacuum in the ***c*** direction, as shown in **Figure 142a**. The unit cell contains a monolayer InSe primary cell, topped by a Ti^{4+} ion. Though multilayer InSe is used in the experiments, the interaction mechanisms between the top Se atoms and the Ti^{4+} ions at the surface are not affected when number of bottom layers is varied in DFT. Hence only monolayer results are reported here.

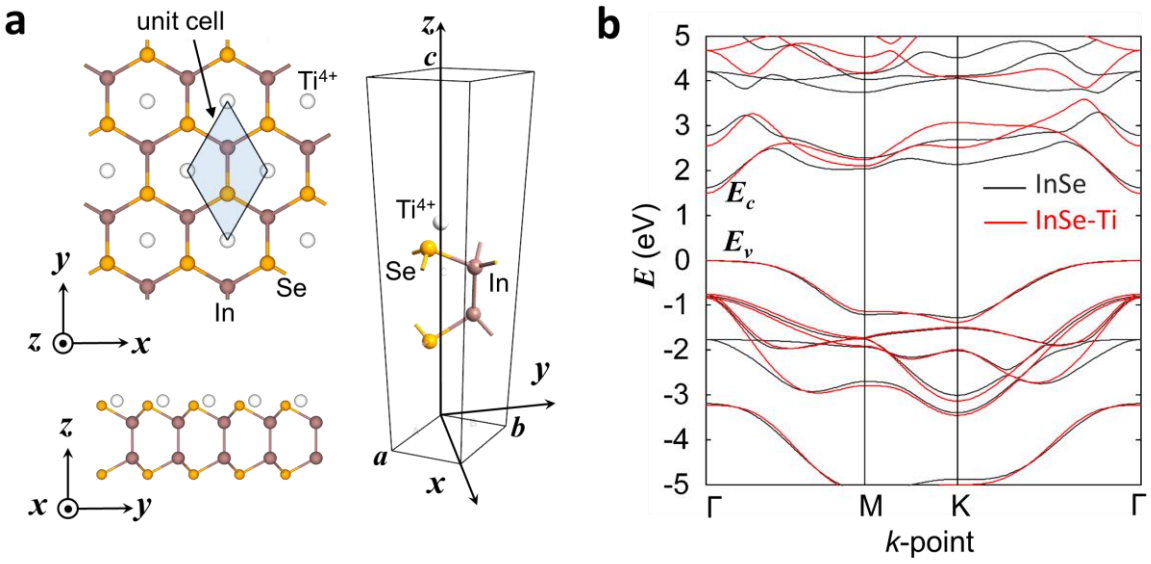


Figure 142: DFT simulation of InSe and InSe-Ti systems.

(a) Unit cell and lattice structure of the InSe-Ti system shown in top view, side view and 3D view. (b) Band structures of InSe and InSe-Ti systems.

Local density approximation (LDA) **[230]** is adopted for the exchange correlations,

together with the double-ζ polarized basis set for expanding electronic density. The intrinsic band structure calculated using this configuration matches previous report very well. **[346]** The calculations are performed using Atomistix ToolKit (ATK) **[242]**. 10×10×1 k-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 75 Rydberg and the maximum force is 0.05 eV/Å for geometry optimization (relaxation). To model the Ti^{4+} ion, atomic compensation charge is applied to take out the four outer orbital electrons from Ti atom and background electron charge is added to neutralize the system.

After relaxation, the each Ti^{4+} ion stays in the center of indium-selenium hexagon, and they do not form Ti-Ti cluster. The crystal structure proposed by simulation is shown in **Figure 142a**, which is consistent with the HAADF results.

The band structures of monolayer InSe and the InSe-Ti system are shown in **Figure 142b**. Valence band maxima is set as zero energy. It can be observed that both systems have a direct band gap at Γ point and the Ti^{4+} ion induces some distortion in the band structures, especially in the conduction band. Atomic Mulliken population **[243]** of each atom is calculated before and after Ti^{4+} treatment (**Figure 143a**), the result of which shows that after Ti^{4+} treatment, 1.037 electrons appear to redistribute in Ti orbitals and the electron population in InSe is decreased by the same amount. This proves the model where the lone pair electrons of Se enter the empty orbitals of Ti^{4+} ion.

3. Results and Discussion

To confirm the formation of coordinate covalent bonds between Ti and Se, bond Mulliken populations (the overlap populations of electrons for pairs of atomic orbitals) are calculated and shown in **Figure 143b**. The population of one Se-Ti pair is $n = 0.323$, which indicates a covalent bond ($n = 0$ and $n > 0$ indicate ionic bond and covalent bond,

respectively). The iso-surfaces of the two eigenstates (real parts) of three surface Se-Ti pairs (a Ti between each of the three Se neighbors) are shown in **Figure 143c** and **Figure 143d** (which are associated to the two eigenvalues of each Se-Ti pair closest to the valence band maxima). The orbital surfaces maintain the 3-fold symmetry of the InSe lattice structure, and the binding can also be confirmed by these overlapped orbitals.

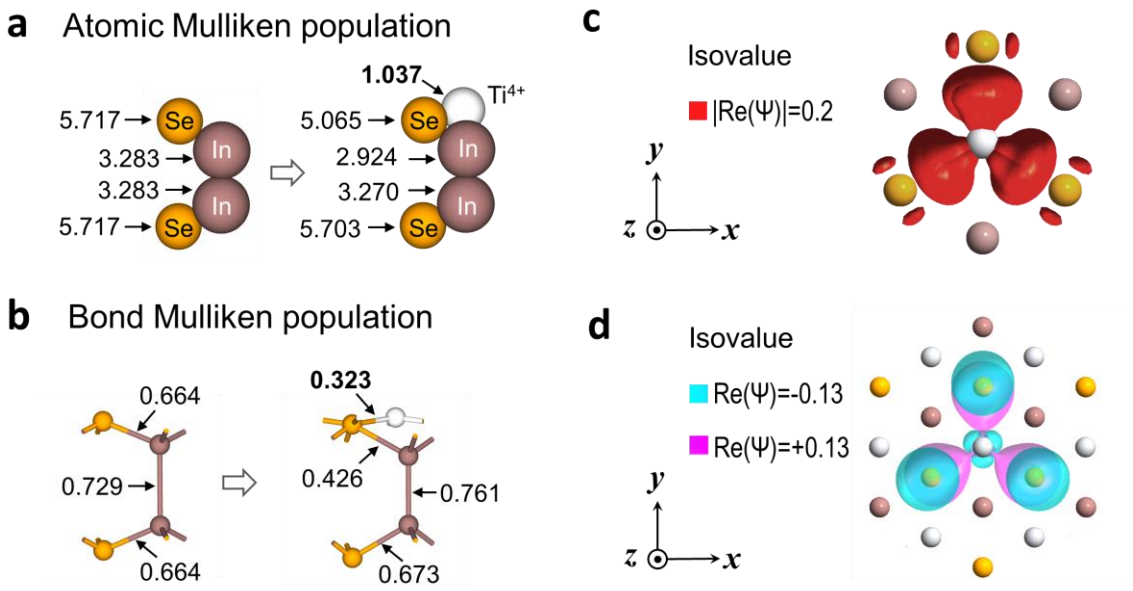


Figure 143: DFT simulation of InSe and InSe-Ti systems (continued).

(a) Atomic Mulliken population of each atom calculated before and after Ti^{4+} treatment. (b) Bond Mulliken population of each pair of atoms calculated before and after Ti^{4+} treatment. (c, d) The iso-surfaces of the eigenstates (real parts) of three surface Se-Ti pairs (the center Ti between each of the three Se neighbors) associated to the (c) first and (d) second eigenvalues below the valence band maxima.

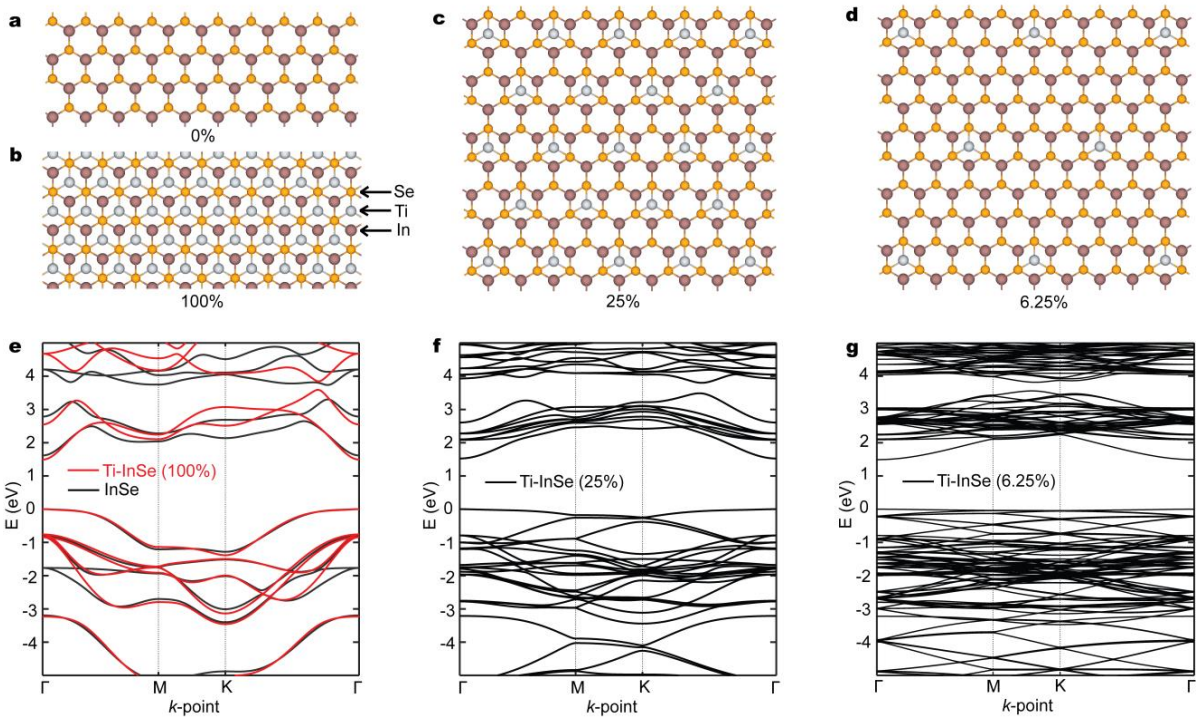


Figure 144: Simulated band diagrams of InSe and InSe-Ti.

(a-d) different Ti coverage rate (0, 6.25%, 25%, 100%). (e-g) band diagrams. The valence band maxima are chosen as energy zero in all the cases. DFT calculations show that both systems have a direct band gap at Γ point. By comparison, it can be observed that the Ti^{4+} ion does not induce trap states in the band gap regardless the coverage rate. Only some distortion is found in the band structures, especially deep in the conduction band. However, the first conduction band valley and the first two valence band peaks at Γ point are nearly not affected. These results show that the electronic properties of InSe are well preserved by the Ti treatment doping, which is more advanced than substitution doping (that degrades the crystal quality). In the band structures of these lower Ti concentrations, we do not observe any localized states either. (Note that the curvatures of the bands change because of the change of Brillouin zone size).

In addition, the band structures of pristine InSe and InSe-Ti complex with different Ti coverage rate (100%, 25% and 6.25%) were calculated. It was found that the additional Ti^{4+} ions do not change the InSe band structure significantly with varying coverage rate (**Figure 144**), it is also worth to notice that even in low coverage, Ti still tend to occupy isolated anchor point, instead of forming cluster. Each system has been relaxed to a maximum force of 0.02 eV/Å, and eventually Ti atoms prefer to stay in the centre of the InSe hexagons rather than cluster, even at lower coverage rate.

F. Band Structure Engineering for Hydrogen Evolution Device

Molybdenum sulfide (MoS_2) has emerged as a promising electrocatalyst for hydrogen evolution reaction (HER) owing to its high activity and stability during the reaction. However, the efficiency of hydrogen production is limited by the number of active sites in MoS_2. In this work, we demonstrate a simple method of fabricating polycrystalline MoS_2 for efficient hydrogen evolution by controlling the Sulphur (S) vacancy concentration, which can introduce new bands and lower the hydrogen adsorption energy. In this section, for the first time, theoretical results show that the HER performance of synthesized MoS_2 with Sulphur (S) vacancy can be further enhanced by the very small amount of Pt decoration which can introduce new gap states and more catalytic sites in real space with suitable free energy. The fabricated hybrid electrocatalyst **[14]** exhibit significantly small Tafel Slope (38 mV/dec) and HER electrocatalytic activity compared to other works. It provides a simple pathway to design low-cost, efficient and sizable hydrogen-evolving electrode by simultaneously tuning the band structure and active sites **[14]**.

1. Introduction

Hydrogen has been widely considered as a promising alternative and renewable energy

to replace fossil fuels **[71]–[73]**. However, the scarcity and high costs of Pt electrocatalysts significantly restrict its applications in large scale. Recently, MoS_2, one of the TMDs, has drawn considerable attention in HER due to the excellent stability and earth abundance **[81]–[85]**. Numerous efforts have been spent to improve the HER performance of MoS_2. Except improving the charge transport of MoS_2 film **[347], [348]**, the most popular method is to create more edges and defects on MoS_2 film **[349]–[354]**. It is known that the edge of MoS_2 is more active for HER electrocatalysts than the inert basal plane **[352]**. Various post-treatment methods **[355]** and vertical MoS_2 structures **[356], [357]** have been developed to expose more edges for efficient HER. In addition to the above strategies, recently, Li et al., reported that the HER performance of CVD-grown monolayer 2H-MoS_2 could be improved by introducing sulfur (S) vacancies and strain **[358]**. The S vacancy and staining the basal plane of MoS_2 can tune the band structure of MoS_2, allowing the reduction of the hydrogen adsorption energy. However, the post treatment for activity sites opening and strain engineering are not practical for large scale application of MoS_2 in HER. Therefore, there is a need of a simple method which can produce MoS_2 with optimal S vacancy concentration. In addition, previous sections have demonstrated that the band structure and electronic properties of MoS_2 can be modified by metal nanoparticles deposited on the surface of MoS_2 **[11]**.

Our collaborators' experimental results **[14]** show that MoS_2 synthesized on the surface of Mo foil by a simple hydrothermal reaction with proper S vacancy concentration can boost the HER performance. (The purpose of usage of Mo as the substrate and Mo source is to form a seamless contact between MoS_2 and Mo substrate, as shown in **Chapter III** that Mo is an excellent contact metal with MoS_2, which can form a high performance contact with MoS_2) The HER performance of synthesized MoS_2 can be further enhanced by the very

small amount of Pt decoration. Pt nanoparticles decorated MoS_2 which is synthesized on Mo foil ($Pt/MoS_2/Mo$) hybrid catalyst demonstrates high HER electrocatalytic activity with low overpotential and small Tafel slope, which is much beyond previous reported works using MoS_2 and is close to the upper-limit values of HER achieved on Pt electrode.

Herein, to explain the experiments, I report a systematic computational study of the high performance HER using MoS_2. DFT simulations show that the very small amount of Pt decoration which can introduce new gap states, thereby lowering the hydrogen adsorption energy, and more catalytic sites in real space with suitable free energy (**Figure 145**).

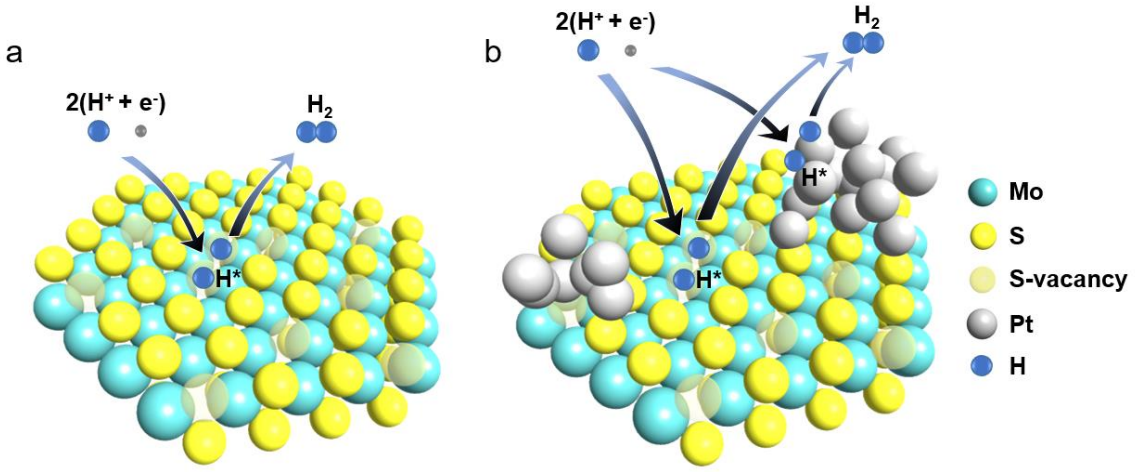


Figure 145. Schematic of HER process on MoS_2 with S-vacancy and Pt.

(a) MoS_2 with S-vacancy, and (b) MoS_2 with S-vacancy and Pt. H* represents H free radical. The HER process has two steps: absorption ($H^+ + e^- \rightarrow H^*$) on catalytic sites and release ($2H^* \rightarrow H_2$) from catalytic sites. Pt nanoparticles provide more catalytic sites for HER.

2. DFT Simulation and Discussion

Density functional theory (DFT) calculation is employed to investigate the influence of the of S-vacancy and Pt atoms on the electronic structure of MoS_2. Since DFT only utilizes periodic boundary conditions with mono-crystalline materials, decorated MoS_2 systems are modeled by a unit cell, which is periodic along lattice vector *a* and *b* and separated by more than 3 nm of vacuum in the *c* direction. All the atoms are allowed to relax.

Local density approximation (LDA) is adopted for the exchange correlations, together with a double ζ polarized basis set for expanding electronic density. The calculations are performed using Atomistix ToolKit (ATK) **[242]**. 4×4×1 k-points are sampled in the Brillouin zone (BZ). The temperature is set to be 300 K. The density mesh cut-off is 75 Rydberg and the maximum force is 0.05 eV/Å for geometry optimizations.

Although the van der Waals (vdW) interaction can be important in weakly bonded systems, such as two-dimensional material systems, however, it is worth noting that it is not necessary to reproduce vdW force in this work. The effect of vdW force is not involved in S-vacancies and is not significant in Pt-MoS_2 interface due to the presence of covalent bonds. Moreover, no significant difference can be observed even if DFT-D2 approach is used to reproduce such nonlocal dispersive force, where a semi-empirical dispersion potential described by a simple pair-wise force field is added to the conventional Kohn-Sham DFT energy.

The band structure of pristine MoS_2 is shown in **Figure 146a**. When an S vacancy is introduced into the MoS_2 crystal structure (3×3 cell), new bands appear in the gap near the Fermi level (red curves) as shown in **Figure 146b**. These new gap states are localized and responsible for hydrogen adsorption and release on the S-vacancies.[28] Hence, S-vacancies are catalytic sites for HER. When Pt atom is introduced (**Figure 146c**), more bands of

localized states appear in the gap. This phenomenon can be observed no matter whether Pt fills the vacancy (**Figure 146c**) or stay on the surface (**Figure 146d**). The increase in the number of gap states results in the strengthening of hydrogen bonding. In addition, Pt nanoparticles themselves also serve as catalytic sites due to their suitable hydrogen adsorption free energy (**Figure 145b**). Therefore, by depositing slight amount of Pt onto MoS_2 surface, HER performance of MoS_2 can be further improved. This method requires very simple preparation process, thereby reducing the fabrication cost.

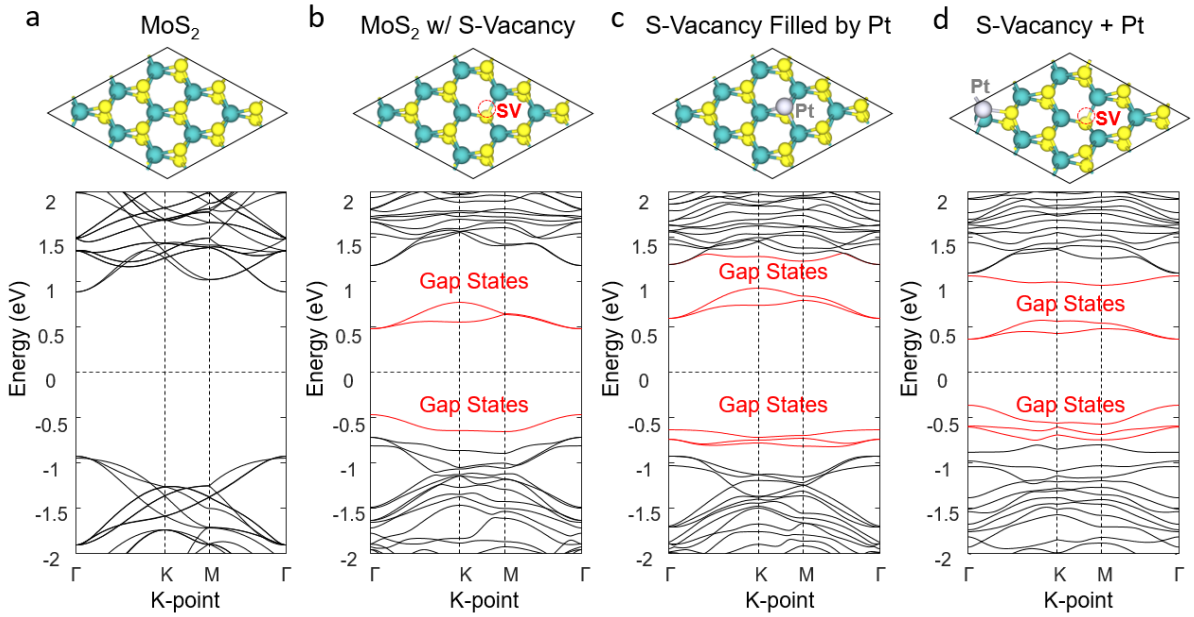


Figure 146. S-vacancies and Pt atom influence on the band structure of MoS_2.

Unit cells (top) and band structures (bottom) of (a) Pristine MoS_2, (b) a 3×3 MoS_2 cell with one S-vacancy, (c) a 3×3 MoS_2 cell with a Pt atom fitting on S-vacancy, and (d) a 3×3 MoS_2 cell with one S-vacancy and a Pt atom sitting on MoS_2 surface.

With the increase of S-vacancy concentration, the bands move closer to the Fermi level and increase the number of gap states (**Figure 147b, c**). These gap states provide more free

energy levels for H* on the catalytic sites, which are lower than that of the intrinsic MoS_2. When the S/Mo is equal to 1.61, a significant number of gap states appear in the gap, and hence many suitable energy levels can be exploited by HER (**Figure 147c**). Moreover, due to the doping effects of the S vacancies, the conductivity of MoS_2 is improved and charges transport more efficiently, thereby enhancing the HER performance.

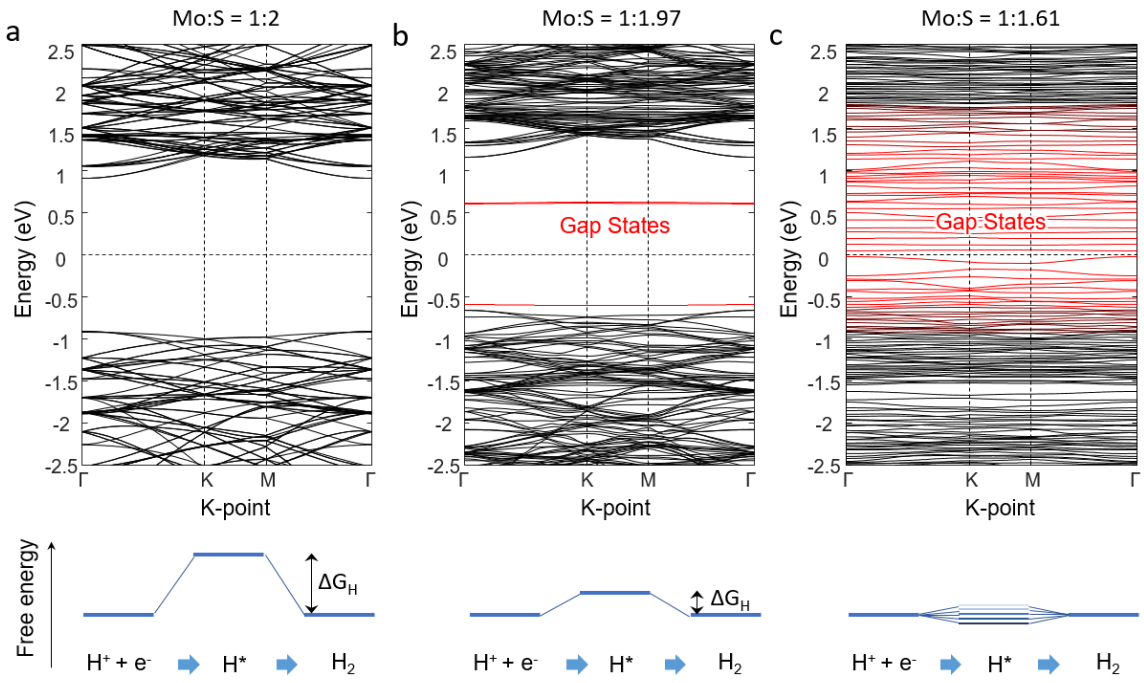


Figure 147. Impact of S-vacancy concentration on MoS_2.

Impact of S-vacancy concentration on the band structure of MoS_2 (upper) and hydrogen adsorption free energy (lower) for (a) a 6×6 cell of pristine MoS_2, (b) a 6×6 cell of MoS_2 with 1 S vacancy, which translates to a Mo:S ratio of 1:1.97, and (c) a 6×6 cell of MoS_2 with 14 random S vacancies, which translates to a Mo:S ratio of 1:1.61. Higher vacancy density provides more catalytic sites with lower free energy levels for H*.

3. Summary of HER of MoS_2

In summary, DFT calculation results show that Sulphur (S) vacancy can introduce new bands in MoS_2, which can lower the hydrogen adsorption energy. Theoretical results indicate that the HER performance of MoS_2 with S vacancy can be further enhanced by the slight amount of Pt decoration which can introduce new gap states and more catalytic sites in real space with suitable free energy. The straightforward and efficient approach makes the MoS_2 films a promising candidate for electrochemical hydrogen production. MoS_2 holds substantial promise for use as an alternative to platinum in electrochemical catalysts to catalyze the hydrogen evolution reaction.

G. Chapter Summary

In this chapter, two representative doping techniques – surface doping and intercalation doping methods are studied.

Using DFT, surface doping by noble metal atoms, nano-particles (such as Ag and Pt), and Lewis acid (Ti^{4+}) have been shown to be a reliable doping method for graphene and MoS_2. Such technique is shown to be useful for various technologies, such as surface functionalization or tuning the threshold voltage of MoS_2 transistors, development of MoS_2 electrocatalyst for HER, as well as improving the conductivity of graphene transparent electrodes.

The studies of intercalation doping of multilayer graphene using Bromine and $FeCl_3$ are presented, so as intercalation doping of MoS_2 using $FeCl_3$, which are shown to be relatively stable, reliable, highly-efficient and practical. The intercalated multilayer graphene can be utilized in various applications – not only transparent electrodes, VLSI interconnects but also on-chip inductors, which will be presented in the next chapter.

VI. Graphene On-Chip Inductors

On-chip metal inductors that revolutionized radio-frequency (RF) electronics in the 1990s suffer from inherent limitation in their scalability in state-of-the-art RF integrated circuits (ICs). This is because the inductance density values for conventional metal inductors, which result from magnetic inductance alone, are limited by the laws of electromagnetic induction. Here we demonstrate a fundamentally different inductor made of intercalated graphene, which uniquely exploits its relatively large *kinetic inductance* and high conductivity to achieve small form-factors and high inductance values that were once thought unachievable in tandem. Our 2-turn spiral inductors based on intercalated graphene exhibit 1.5-folds higher inductance density leading to one-third area reduction compared to conventional inductors, while providing undiminished *Q*-factors up to 12. This purely material-enabled technique provides an attractive solution to the longstanding scaling problem of on-chip inductors and opens up an unconventional pathway for the development of future ultra-compact wireless communication systems.

A. Background – On-Chip Inductors

1. On-Chip Inductors in RF-ICs

Inductor – a passive component in an electric circuit that possesses inductance, is used to store electrical energy in a magnetic field when electric current is flowing through it. Inductors are widely used in alternating current (AC) electronic circuits, particularly in radio frequency (RF) applications. They can be used to block AC while allowing direct current (DC) to pass, or used in electronic filters to separate signals of different frequencies. They can also be used in combination with capacitors to make tuned circuits that generate or receive signals of specified frequencies. An inductor is characterized by its inductance (*L*),

which is the ratio of the voltage (V) to the rate of change of current (dI/dt). Thus, $V = -L\,dI/dt$, where the negative sign indicates that the induced voltage is in a direction that opposes any change in the current.

On-chip inductors are devices that are integrated into semiconductor integrated-circuit (IC) chips. They can be realized using Back-End-of-Line (BEOL) CMOS technology similar to on-chip interconnects. They are widely used in RF ICs and are one of the performance as well as cost limiting elements of RF ICs.

Then the question arises, why on-chip inductors are used for RF applications instead of "off-chip" (external) inductors. For relatively low-frequency applications below a few GHz, off-chip inductors can be connected externally with the RF chip, since the inductance values needed are typically large (in the μH-scale) and implantation of such large inductors as concrete components is simple. However, as the frequency increases, the inductance values needed become relatively small. For example, modern RF circuits such as a voltage-controlled oscillator (VCO) working in super high frequency (SHF) band (3 – 30 GHz) or extremely high frequency (EHF) band (30 – 300 GHz) typically need an inductance on the order of nH. However, the parasitics (in the connection to the external inductors), especially the inductance associated with the package pin and bond wire, can exceed 1 nH **[359]**, which can even overwhelm the needed inductance values. Hence, it's impossible to access such a small inductance externally. As a result, on-chip inductors are commonly used in RF applications such as low-noise amplifiers (LNA), mixers and oscillators (**Figure 148**), which can be found in various kinds of transmitters, receivers or transceivers. Moreover, integration of on-chip inductors can eventually lower the cost of manufacturing and minimize the sizes of the RF systems.

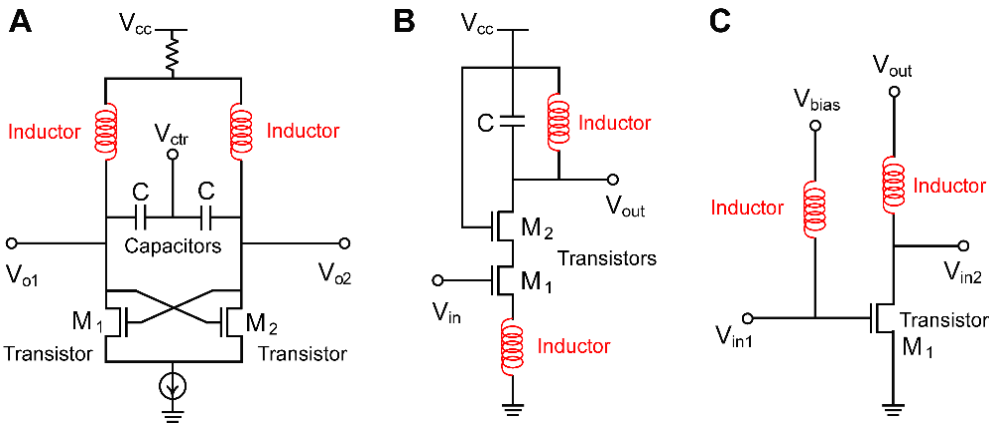


Figure 148: Schematic of a typical (A) VCO, (B) LNA and (C) frequency mixer. On-chip inductors form essential components of these circuits.

2. Chip Area Occupied by Inductors

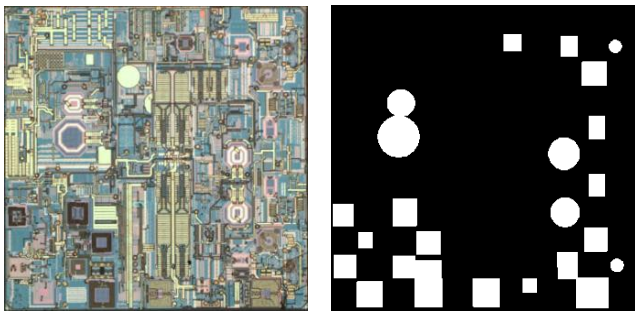


Figure 149: QUALCOMM WTR4905.

Left: Die photo of QUALCOMM WTR4905 used in iPhone 7Plus. Right: pixel image of the die photo on the left where white areas are inductors.

In ICs the on-chip inductors occupy significant area. Moreover, inductor sizes do not scale with process geometry as discussed in the next section. This limits the potential for down scaling the size of the chip, and has a concomitant cost implication. Generally all the passive components together (resistors, capacitors, inductors, etc.) may take up to 70-80% of chip area. Besides, inductors may take up to 70-80% of area in sub-circuits like LNAs or

VCOs. However, giving concrete numbers about how much chip area is occupied by on-chip inductors is impossible, because purpose, design and technology vary from chip to chip. In this section, we estimate that planar on-chip spiral inductors could occupy up to 50% of the area of most RF IC chips.

Although the designers avoid inductors as much as possible, the commercial RF ICs, for example, transceivers can still contain tens of inductors that still take a large portion of the chip area. As shown in the example below (**Figure 149**), there is the newest and very optimized LTE transceiver IC (WTR4905) used in iPhone **[360]**, where there are still more than 20 inductors and the total area of those inductors is more than 15% of the chip area, according to our calculation based on pixel statistics. Moreover, in the RF chips in the WIFI module employed in iPhones **[361]**, the inductors take up nearly 20% of the area according to our statistics. Other examples illustrated below (**Figure 150**) highlight state-of-the-art RF chips reported in papers published in the prestigious IEEE International Solid-State Circuits Conference (ISSCC) during 2014 − 2016, based on modern techniques. We note that the total area of inductors can even take up more than 40% of the main chip area, according to our calculation based on pixel statistics (**Table 11**). This number may even be higher in less optimized RF chips. Hence, it is reasonable to say that on-chip inductors can occupy "up to 50% of the area".

Decrease in die area translates into more dies fabricated on a wafer, which in turn implies a lower die cost. For an RF chip with 40% area taken by inductors, if the inductor area can be reduced by a factor of 2 (equivalent to 20% reduction), according to **[362]** (die cost $\propto$ area $\times$ (1 + area $\times$ defect density)), we can estimate that a chip area reduction of 20% results in a cost reduction of approximately 23%, for a die area of 1 cm^2 and defect density of 0.222/cm^2.

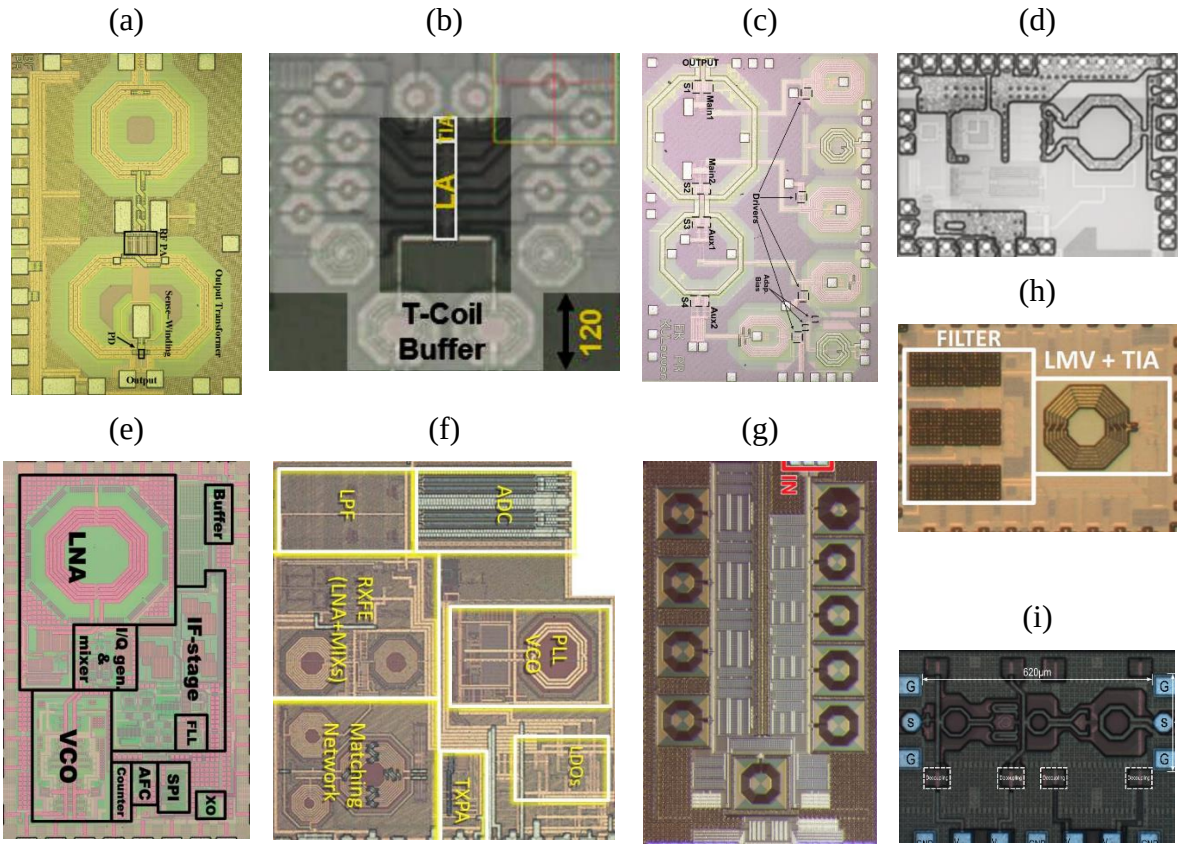


Figure 150: Die photos of some RF-ICs from ISSCC.

(a) A Transformer-Coupled True-RMS Power Detector in 40 nm CMOS [363]. (b) A 28Gb/s 1pJ/b Shared-Inductor Optical Receiver in 28nm CMOS [364]. (c) A Dual-Mode Transformer-Based Doherty LTE Power Amplifier in 40 nm CMOS [365]. (d) A 3G/4G CMOS Power Amplifier [366]. (e) A 227 pJ/b -83dBm 2.4 GHz Multi-Channel OOK Receiver Adopting Receiver-Based FLL [367]. (f) A 6.3 mW BLE Transceiver Embedded RX Image Rejection Filter and TX Harmonic-Suppression Filter Reusing On-Chip Matching Network [368]. (g) A Dual-Frequency 0.7-to-1.0 GHz Balance Network for Electrical Balance Duplexers [369]. (h) A 600 µW Bluetooth Low-Energy Front-End Receiver in 0.13µm CMOS Technology [370]. (i) A 28 GHz Efficient Linear Power Amplifier for 5G Phased Arrays in 28 nm Bulk CMOS [371].

Table 11: Chip area taken by on-chip spiral inductors in advanced commercial and state-of-the-art RF IC chips.

Category	Chip Name/Description	CMOS Process	Frequency /Band	Inductor Area	Refer-ence
Modern Commer-cial RF ICs	A Multimode RF transceiver optimized for the volume tier (Qualcomm WTR4905)	28 nm	LTE Cat6	15.1 %	**[360]**
	A Band Pass Filter 2.4 GHz in iPhone Wi-fi module	n/a	2.4 GHz/ Wi-fi	17.8 %	**[361]**
	A Front End Module 2.4 GHz in iPhone Wi-fi module	n/a	2.4 GHz/ Wi-fi	14.9 %	**[361]**
	A Skyworks 5 GHz Power Amplifier in iPhone Wi-fi module	n/a	5 GHz/ Wi-fi	13.3 %	**[361]**
State-of-the-Art RF IC Chips reported in ISSCC During 2014-2016	A Transformer-Coupled True-RMS Power Detector in 40 nm CMOS	40 nm	5GHz/ WLAN	41.8 %	**[363]**
	A 28 Gb/s 1pJ/b Conventioanl-Inductor Optical Receiver in 28 nm CMOS	28 nm	n/a	36.9 %	**[364]**
	A 28 Gb/s 1pJ/b Shared-Inductor Optical Receiver in 28 nm CMOS	28 nm	n/a	43.4 %	**[364]**
	A Dual-Mode Transformer-Based Doherty LTE Power Amplifier in 40 nm CMOS	40 nm	1.9 GHz	38.1 %	**[365]**
	A 3G/4G CMOS Power Amplifier with Polar Antenna Impedance Detection and Tuning for Efficiency Improvement	0.13 μm	1.95 GHz/ 3G/4G	22.1 %	**[366]**
	A 227pJ/b -83dBm 2.4 GHz Multi-Channel OOK Receiver Adopting Receiver-Based FLL	65 nm	2.4 GHz	29.3 %	**[367]**
	A 6.3 mW BLE Transceiver Embedded RX Image Rejection Filter and TX Harmonic-Suppression Filter Reusing On-Chip Matching Network	40 nm	2.4 GHz	16.8 %	**[368]**
	A Dual-Frequency 0.7-to-1.0 GHz Balance Network for Electrical Balance Duplexers	0.18 μm	0.7-1 GHz	28.6 %	**[369]**
	A 600 μW Bluetooth Low-Energy Front-End Receiver in 0.13 μm CMOS Technology	0.13 μm	2.4 GHz/ Bluetooth	15.8 %	**[370]**
	A 28 GHz Efficient Linear Power Amplifier for 5G Phased Arrays in 28 nm Bulk CMOS	28 nm	28 GHz	25.2 %	**[371]**
	A Scalable 28 GHz Coupled-PLL in 65 nm CMOS with Single-Wire Synchronization for Large Scale 5G mm-Wave Arrays	65 nm	28 GHz	20.5 %	**[372]**
	A 68.1-to-96.4 GHz variable-gain low-noise amplifier in 28 nm CMOS	28 nm	68.1-96.4 GHz	22.9 %	**[373]**
Older RF ICs	A UHF Proximity Micro-Transceiver for Mars Exploration	n/a	400 MHz	35.1 %	**[374]**
	A 200 MHz 1-pole on-chip bandpass filter	2.0 μm	200 MHz	50.0 %	**[375]**

It is worth noting that for applications with off-chip inductors, such as RF IDs, the area ratio of inductor:chip can be huge (as shown in **Figure 151**), meaning that the size of the ID tag is dominated by the inductor. The technique demonstrated in this work can also be an approach to minimize the form-factor and cost of such applications without performance loss.

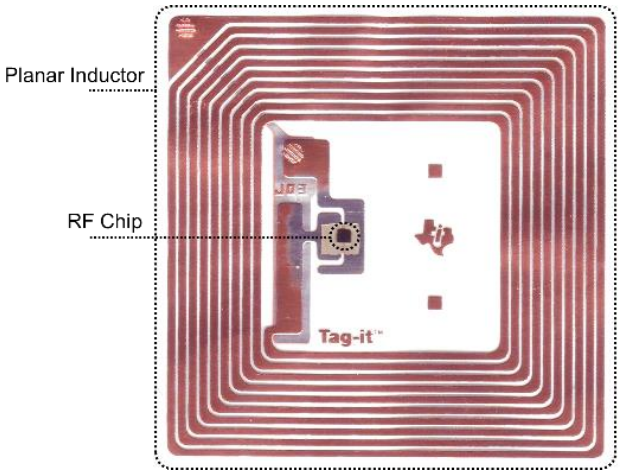


Figure 151: A typical RF ID with a large planar inductor and a small RF chip.

3. Scaling Trend of On-Chip Inductors

Compared to the continuous scaling of transistors and interconnects in the IC technology achieved with increase in performance, scaling of on-chip inductors is slower due to the fact that large inductor areas, dictated by fundamental electromagnetics, are required in order to deliver the desirable inductance values and performance targets. Although the need of inductance values can be reduced by circuit design and optimization **[376]**, however, the area required for each on-chip inductor still scales slower than that of active devices and interconnects, as shown in **Figure 152**.

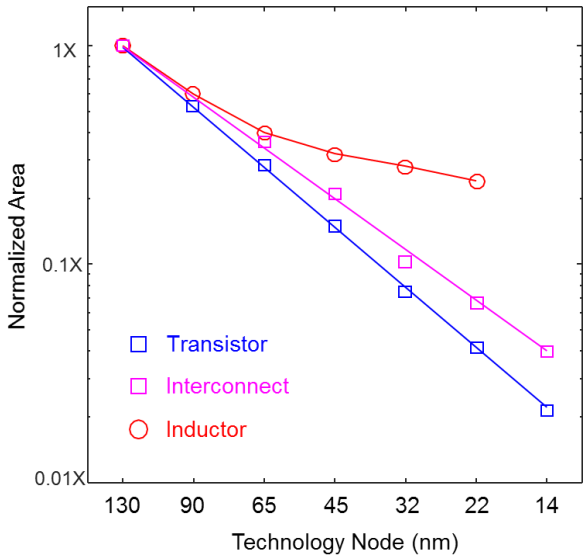


Figure 152: Comparison of scaling trends.

Required area of a typical on-chip inductor [376] vs. area of a single logic transistor (= gate pitch × metal pitch) [377]–[384] and width^2 of M1 interconnect [377]–[384]. Data are normalized w.r.t the 130-nm node.

A more detailed calculation for a specified voltage controlled oscillator (VCO) is presented in **Figure 153**. The parameters for each technology node are obtained from the International Technology Roadmap for Semiconductors (ITRS) tables **[50]**, including cut-off frequency (f_T), gain, gate capacitance and dimensions of the RF transistors. The maximum working frequency of the VCO is then determined by $f_T/10$. Hence, using $f_T/10=1/2\pi\sqrt{LC}$, the value of L needed by each node can be estimated. The maximum allowed series resistance R for the inductors is then determined by the negative resistance ($|R_{in}|$) provided by the differential pair. Using the values of L and R, the inductor area required by each node can finally be estimated using the analytical models.

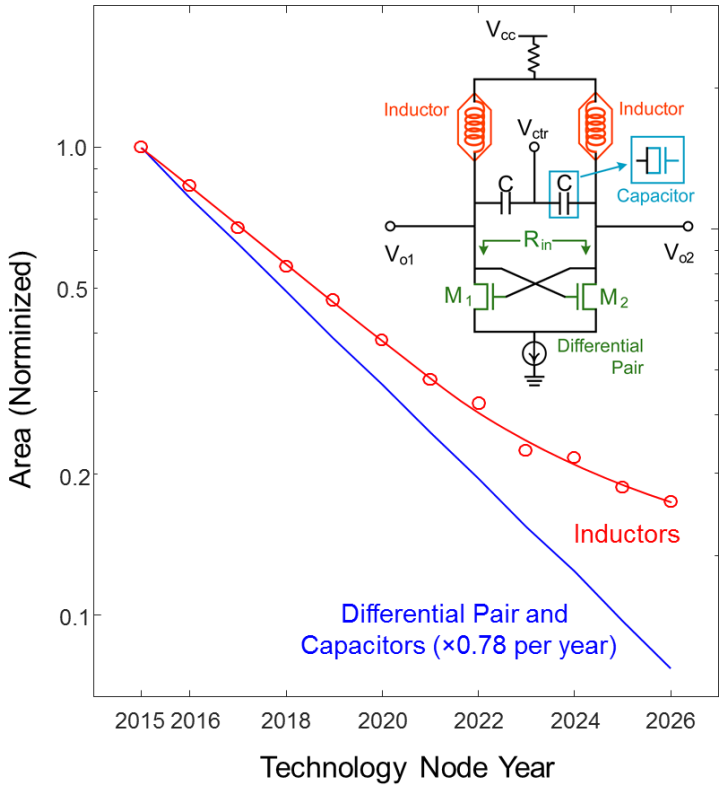


Figure 153: Comparison of scaling trends.

Required area of on-chip inductors in a VCO *vs.* area of other circuit components, calculated based on ITRS data. Data are normalized w.r.t the 2015 node.

4. The Physics of Magnetic Inductance and Kinetic Inductance

In general, inductance is the property of a conductor by which a change in current through it induces an electromotive force (emf) in both the conductor itself and in any nearby conductors.

According to Faraday's law of electromagnetic induction, a change in current over time (t) through a conductor induces a change in magnetic field and thus magnetic flux (Φ_B) (**Figure 154A**), resulting in an emf (= - $d\Phi_B / dt$) in both the conductor itself and in any nearby conductors. This effect is the magnetic inductance (L_M), and the effect in the

conductor itself is named self-inductance (L_{Self}) while in nearby conductors it is named mutual inductance (L_{Mutual}). The relationship between the self-inductance of a conductor, the voltage, $u(t)$, and the current, $i(t)$, through the conductor is $u(t) = - L_{Self} \, d \, i(t) / dt$,, while for mutual-inductance, the voltage in conductor/loop 2 is $u_2(t) = - L_{Mutual} \, d \, i_1(t) / dt$, where $i_1(t)$ is the current in neighboring conductor/loop 1 (**Figure 154B**). The magnetic field energy E stored in an inductor can be calculated as $E = ½ \, L_M \, i^2$.

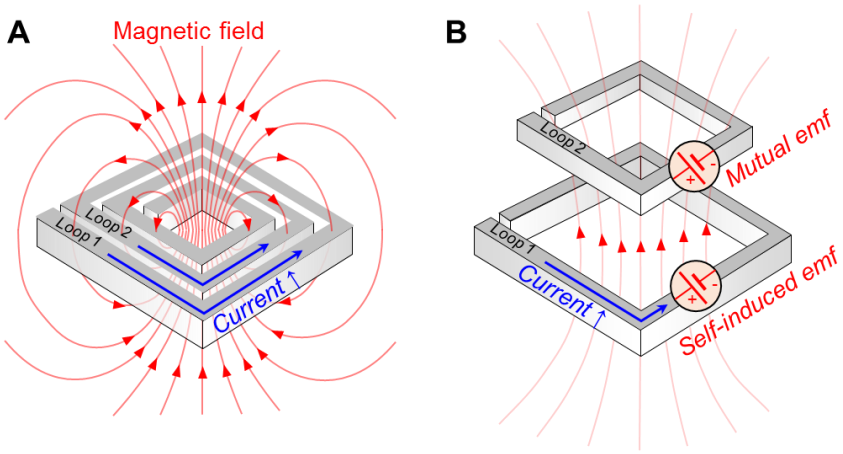


Figure 154: The physics of magnetic inductance.

(A) Illustration showing the relation between the current and magnetic field in an on-chip inductor. (B) Illustration highlighting self and mutual inductance. Current in the outer conductor (loop 1) is assumed to be increasing causing the magnetic flux through itself and through the inner conductor (loop 2) to increase. Hence, the induced emf in both conductors are in a direction that opposes that change (Lenz's Law).

In short, L_M is defined by the magnetic flux change induced by a change in current. Since the amount of magnetic flux is proportional to the "surface area" of the coils, certain inductor size and area are required in order to deliver the desirable inductance values and operation frequency (the working frequency at which the performance is the best) required

by circuit design, as illustrated in **Figure 155**. Hence, inductor devices based on magnetic inductance cannot be scaled in the way of transistor or interconnect scaling.

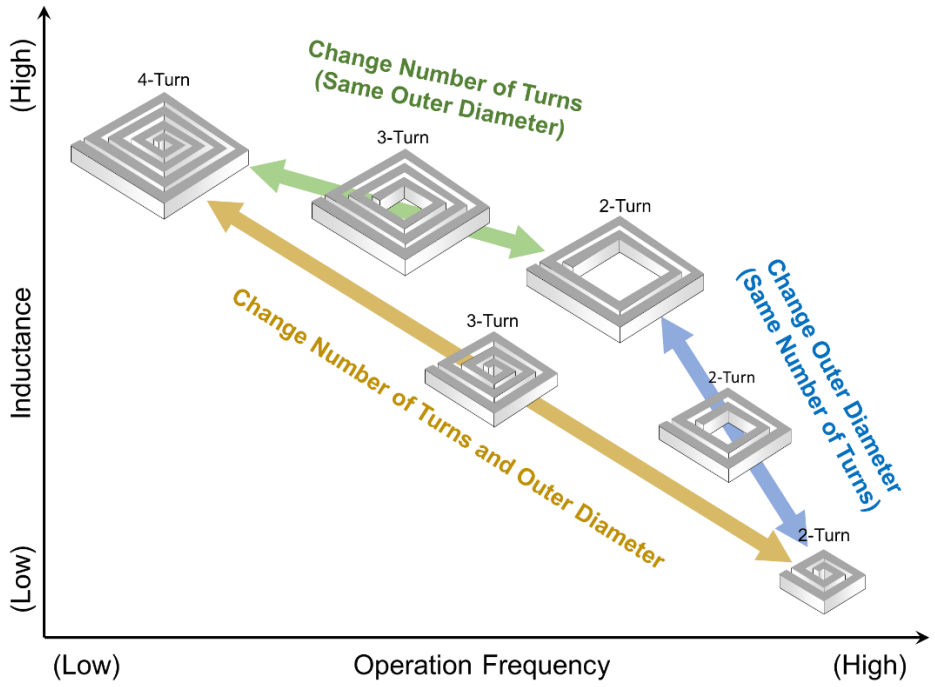


Figure 155: Effects of outer diameter and number of turns.

Illustration showing how inductance and operation frequency change qualitatively with outer diameter (area) and number of turns.

Kinetic inductance L_K is the manifestation of the inertial mass of mobile charge carriers in alternating emf as an equivalent series inductance. The "inertia" of charge carriers is described by the fact that the charge carriers, like all objects with mass, prefer to be traveling at a constant velocity and therefore it takes a finite time to accelerate the particle and change the emf (**Figure 156**). This is similar to how the finite rate of change of magnetic flux affects the change in emf. Since this portion of emf is irrelevant to the magnetic field inside/around the spiral, L_K is only dependent on the momentum relaxation as

well as the conducting channels in the material and hence, not dependent on the inductor area. Due to the irrelevance to the magnetic field, there is no mutual kinetic inductance.

Hence, the total inductance of a conductor can be calculated as: $L_{total} = L_M + L_K = (L_{Self} + L_{Mutual}) + L_K$.

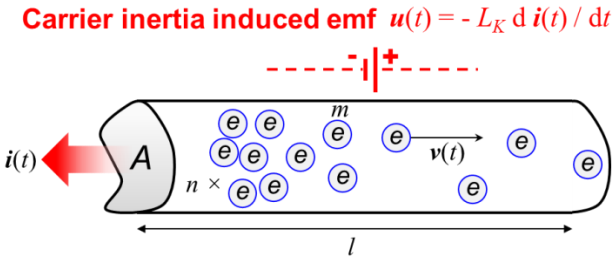


Figure 156: Schematic of a conductor wire showing the source of kinetic inductance.

The kinetic inductance L_K of a conductor wire can be calculated using kinetic energy E_K:

$$E_K = \tfrac{1}{2} M v^2 \tag{29}$$

where M is total mass of carriers, v is velocity of carriers (**Figure 156**). Now,

$$M = m^* n (A l) \tag{30}$$

where m^* is mass of single carrier, n is carrier density, A is cross sectional area of material and l is length of conductor (**Figure 156**). Also, current, $i = A (n e v)$. Hence,

$$v = i /(A n e) \tag{31}$$

Using **Equation 30** and **Equation 31**, in **Equation 29**:

$$E_K = \tfrac{1}{2} (m^* n A l) (i /A n e)^2 \tag{32}$$

Thus, E_K per unit length is $\tfrac{1}{2} (m^* / A n e^2) i^2$. Comparing this to magnetic energy stored in an inductor $E = \tfrac{1}{2} L i^2$, we get:

$$L_K = (m^* / A n e^2) \tag{33}$$

Due to low carrier densities (n), L_K tends to be significantly large in low-dimensional materials. Using the frequency-independent dc conductivity $\sigma_0 = n_{1D}\, e^2\, \tau / m^*$ (where n_{1D} is the one-dimensional carrier density), kinetic inductance component over frequency for a single 1-D conducting channel (i.e., in carbon nanotubes or graphene nanoribbons) can be calculated as $j\omega L_K = j\omega\, \tau / \sigma_0$ **[58]**, where ω is the angular frequency, and τ is the momentum relaxation time, defined by $\tau = \lambda / 2\upsilon_F$, where λ is the mean free path and υ_F is the Fermi velocity.

Kinetic inductance is negligibly small in conventional metals. This is due to two reasons. First, the momentum relaxation time for a metal is usually very small (on the order of 10^{-14} s) **[385]**, and thus, $j\omega L_K = j\omega\, \tau / \sigma_0$ is negligible for frequencies less than a terahertz ($\omega\tau < 1$). Moreover, the total kinetic inductance also scales down with the number of conducting channels N (as will be shown later), which is usually very large for metals, unless for extremely small dimensions where they are either thermodynamically unstable and/or unreliable from a current-carrying capacity perspective **[15]**. Whereas, the momentum relaxation time for carbon nanomaterials (i.e., carbon nanotubes or graphene ribbons) is on the order of 10^{-12} s, or even larger, and the conducting channel number N is small. Hence, one can observe a significantly large kinetic inductance in carbon nanomaterials. For example, for a single conducting channel in a carbon nanotube or a graphene nanoribbon, L_K per unit length is about 8 nH/μm **[57], [58]**.

Because of the insignificance of L_K in conventional metals compared to L_M, in the past few decades, almost all the studies on the inductance value improvements of on-chip inductors have been focused on the structural improvements, as discussed in the main text. However, if the significantly larger kinetic inductance in carbon nanomaterials can be exploited in inductors, one can harvest more total inductance, in addition to any L due to

structural improvements alone. Moreover, the presence of large kinetic inductance can also reduce the skin effect (describing the phenomenon that at high frequencies, the current flow concentrates near the outer surfaces of conductors, and therefore the resistance increases significantly, while inductance decreases with the frequency) of the inductors, since high values of L_K makes the total "self-inductance" (= $L_{self,\ \text{magnetic}} + L_K$) of the individual conductor segments significantly larger than their mutual inductance values **[58]**. As a result, the current has no incentive to flow through the segments near the perimeter of the conductor cross section to lower the total inductance at higher frequencies.

5. Equivalent Circuit Models for On-Chip Inductors

Figure 157A shows the schematic view (cross-section) of an on-chip spiral inductor structure, using intercalated multilayer graphene (MLG) as an example, where the parasitics of the structure are marked. L_M, L_K and R_S are the magnetic inductance (self+mutual), kinetic inductance, and series resistance of intercalated MLG, respectively. C_s, C_{ol}, C_{ox}, C_{sub}, and R_{sub} represent the inter-turn coupling capacitance, overlap capacitance, substrate dielectric capacitance, substrate capacitance and resistance, respectively. $R_{c1,2}$ and $C_{c1,2}$ represent the contact resistance and capacitance, respectively. Eddy inductance and resistance, L_{eddy} and R_{eddy}, capture the eddy current effects in the substrate. Note that for the fabricated MLG inductors in this work, transparent quartz substrates were used, which is very thick, in order to minimize the substrate loss. When measuring those devices, the substrate plate is the probe station platform beneath quartz.

Figure 157B and **Figure 157C** show the full and simplified equivalent circuit models, respectively.

The value of L_M can be estimated by analytical models, in two parts $L_{Self} + L_{Mutual}$. L_{Self} has the analytical form of **[386]**:

$$L_{Self} = \sum_n 2l_n \left[\log\left(\frac{2l_n}{w+t} \right) + 0.5nH + \frac{w+t}{3l_n} \right] \quad (34)$$

where n is the index of each straight segment in the spiral, l_n is the length of segment n, w and t are the width and thickness of the spiral, respectively. For example, for the first segment, l_1 equals D, the outer diameter, while for the sixth segment, $l_6 = D - 2w - 2s$, where s is the space between two turns and w is the width of the spiral (**Figure 157D**). L_{Mutual} has the analytical form of **[386]**:

$$L_{Mutual} = 2nH/cm \sum_{m,n} S \left\{ \begin{array}{l} l_+ \left[\log\left(\frac{l_+}{d} + \sqrt{1+\frac{l_+^2}{d^2}} \right) - \sqrt{1+\frac{l_+^2}{d^2}} + \frac{l_+}{d} \right] \\ \qquad - l_- \left[\log\left(\frac{l_-}{d} + \sqrt{1+\frac{l_-^2}{d^2}} \right) - \sqrt{1+\frac{l_-^2}{d^2}} + \frac{l_-}{d} \right] \end{array} \right\} \quad (35)$$

where m and n are the index of two segments, d is the distance between the centers of segments m and n, $l_+ = (l_m + l_n)/2$, $l_- = (l_m - l_n)/2$, and S is +1,-1 or 0 if the current directions in the two segments are parallel, opposite, or orthogonal.

As shown in the example in **Figure 158**, a comparable L_K (if it exists) w.r.t. L_M, can significantly improve both the inductance and the quality factor (Q-factor). Q-factor can be regarded as a measure of the ratio of the desired quantity, related to the inductive reactance (= ωL),to the undesired quantity (resistance). For an ideal inductor with only series inductance L and resistance R_S but no capacitance, its Q-factor is given by $\omega L/R_S$, i.e., linear w.r.t frequency, as shown by the green dash line (1) in **Figure 158**. In reality, the Q-factor of an inductor will not be that linear with frequency due to the existence of capacitive parasitics. Hence, the ideal Q-factor ($\omega L/R_S$) serves as an upper bound of the Q-factor.

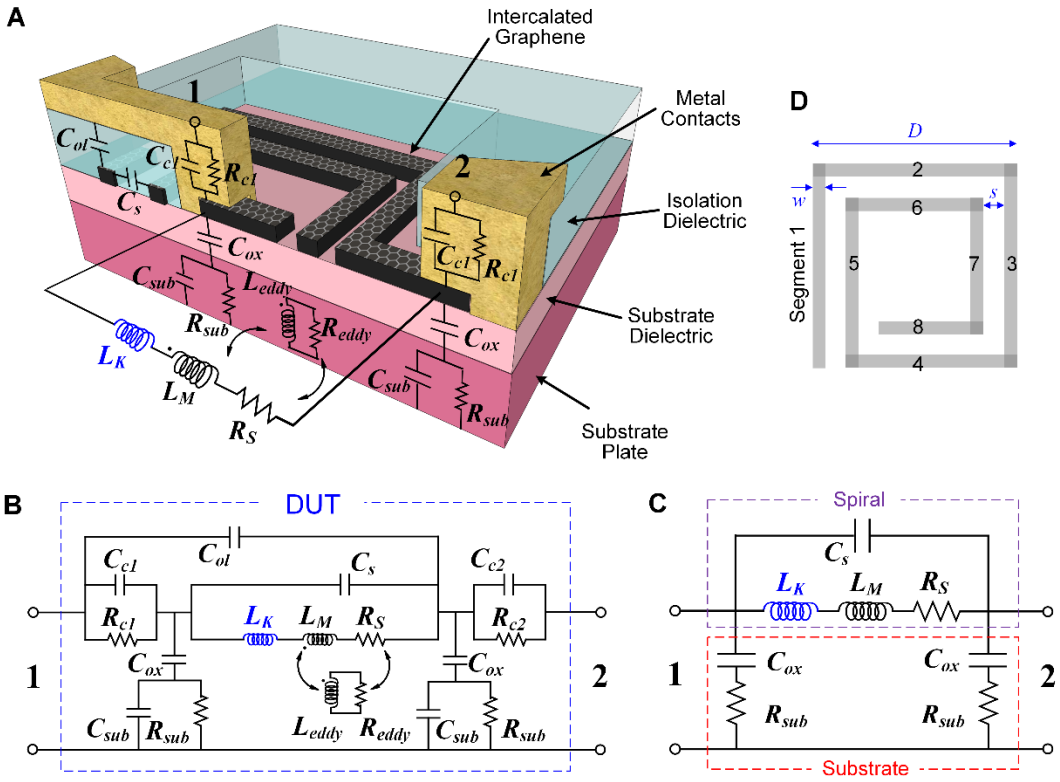


Figure 157: Equivalent circuits of intercalated MLG inductor.

(A) Schematic view of intercalated MLG on-chip spiral inductor with the equivalent circuit parameters. (B) Equivalent circuit model for the device under test (DUT) in (A), which is a two-port network. (C) A simplified equivalent circuit model from (A), where only the key parasitics due to the spiral and substrate are shown, while other minor parasitics are neglected. (D) An example inductor layout highlighting the dimensions and the segment indices. *D* represent the diameter; *s* is the space between two turns and *w* is the width of the spiral.

At low frequencies, *Q*-factor usually follows the trend of $\omega L/R_S$. At higher frequencies, *Q*-factor starts to decrease, as shown by the red and blue curves as well as the green dash line (2) in **Figure 158**, mainly due to three effects:

The first is the substrate loss, which describes the effect that as frequency increases,

capacitive and magnetic coupling with substrate become more and more significant. The rate of decrease of Q-factor due to this effect is roughly $C_{ox}R_{sub}/\omega$.

The second effect is the self-resonance: as the frequency increases, the inter-turn parasitic capacitance of the inductor becomes more and more dominating, which reduces Q-factor. At the frequency where Q-factor drops to zero, those parasitic capacitances form a parallel resonance with the inductance L and the inductor becomes a tuned circuit. Such frequency is named self-resonant frequency (SRF), and can be calculated as $1/(2\pi\sqrt{LC_s})$. Typical inductor operation is therefore designed to be far from the SRF.

The third effect, the skin effect of the conductor, describing the phenomenon that at high frequencies, the current flow concentrates near the outer surfaces of conductors, and therefore the resistance increases significantly while inductance decreases with the frequency. The skin effect can be characterized by the skin depth δ, defined as the depth below the surface where the current density falls to $1/e$ (≈ 0.37) of that of the surface. The skin depth is proportional to $f^{-0.5}$ and is calculated as $\delta = [\rho / (\pi\mu f)]^{0.5}$, where ρ and μ are the resistivity and the absolute magnetic permeability of the metal **[387]**. The skin effect can become very significant in Cu inductors working at frequencies over 100 GHz, where the skin depth (< 200 nm) is less than the inductor segment dimensions. In fact, the onset of skin effect is defined as $\delta = \frac{1}{2} \min\{w, t\}$, i.e., when the skin depth equals half the value of the smaller of the conductor width (w) or thickness (t).

Note that in **Figure 158**, **Equations 34** and **35** are used. The ratio of w:s:D:t is kept as 20:5:100:1 when the area (D^2) is scaled. Other assumptions include a SiO_2 substrate dielectric of 100 μm, a Si substrate with conductivity of 4×10^4 S/m^2, and a SiO_2 top dielectric of 2 μm.

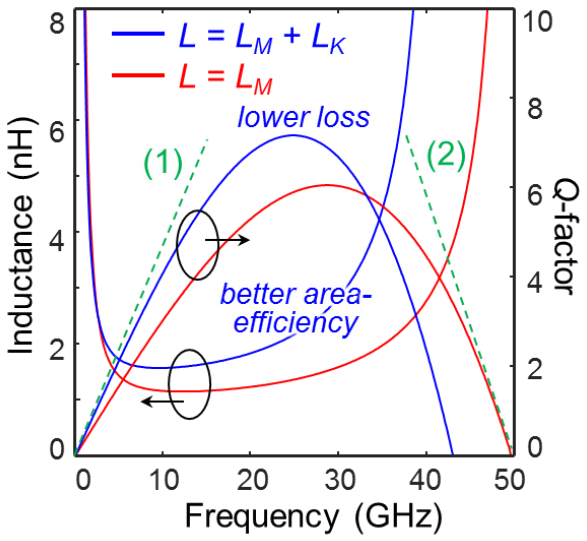


Figure 158: Plots of total inductance and *Q*-factor vs. frequency.

The plots are calculated using the circuit model in (B), assuming L_M = 1 nH, R_S = 20 Ω and C_S = 10 fF. In the case with L_K, L_K is assumed to be 40% of the value of L_M, which is typically in the nH-scale. Underlying substrate is assumed to be identical for both cases. Green dash lines represent (1) the $\omega L/R_S$ upper limit of *Q*-factor, and (2) the substrate loss, self-resonance and skin effects at high frequencies.

6. Summary of Current Inductor Techniques

The emerging paradigm of *Internet of Things* (IoT) will require tremendous amount of miniaturized wireless connections to be enabled by radio frequency integrated circuits (RF-ICs) with scalability, flexibility, high-performance and ease of integration. Moreover, the market value of radio frequency identification (RF-ID) that employs electromagnetic fields to automatically identify and track tags attached to objects is expected to rise to US$18.68 billion by 2026 **[388]**. As discussed previously, as essential passive devices in RF-ICs, planar on-chip metal inductors can occupy up to 50% of the chip area, and also contribute a

major part of the form factor of RF-IDs (**Figure 151**). However, unlike the continuous scaling of transistors and interconnects in the IC technology achieved with increase in performance, progress toward miniaturization of on-chip inductors has remained elusive mainly due to the fact that large inductor areas, dictated by fundamental electromagnetics, are required in order to deliver the desirable inductance values and performance targets, as shown in **Figure 152**, **Figure 153**, **Figure 154** and **Figure 155**.

To achieve the continuous size scaling while fulfilling the inductance and performance requirements, improvement in the inductance density (inductance to area ratio) is essential, which is defined by inductance per unit area = total inductance (L_{total}) / inductor area, where L_{total} is the sum of *magnetic inductance* (L_M) and *kinetic inductance* (L_K). The *magnetic inductance* relies on the magnetic field and is determined by the structural design of the inductor, while *kinetic inductance* relies on the inertial mass of carriers and is purely a material property. Therefore, *structural design* and *materials innovation*, that determines L_M and L_K, respectively, are two simultaneous ways to improve inductance density. As shown in the example in **Figure 158**, a comparable L_K (if it exists) w.r.t. L_M, can significantly improve both the inductance and the quality factor (*Q*-factor, or *Q*). However, because in conventional metals L_K is negligibly small (because of relatively weak carrier inertia) compared to L_M, almost all the studies in the past few decades have been focused on the structural improvements to make full use of the magnetic field, such as layout optimization **[389]**, micro-electromechanical-system fabrication **[390], [391]**, 3D self-rolled-up **[392]**, vertical-stacked **[393], [394]** architectures and magnetic cores/dielectrics **[395], [396]**.

B. Multilayer Graphene (MLG) On-Chip Inductors

Theories have identified that carbon nanomaterials including carbon nanotube bundles and multilayer graphene (MLG) can be a very attractive material-based approach for on-chip

inductors **[58], [59]**, because the large momentum relaxation time (τ) of low-dimensional carbon allotropes could lead to large L_K in typical on-chip inductor sizes, which can be comparable to L_M, thus contributing to high area-efficiency and performance, as well as immunity to skin effect **[60], [61]**. Using MLG also ensures that the large quantum contact resistance of monolayer graphene can be lowered to acceptable values **[61]**.

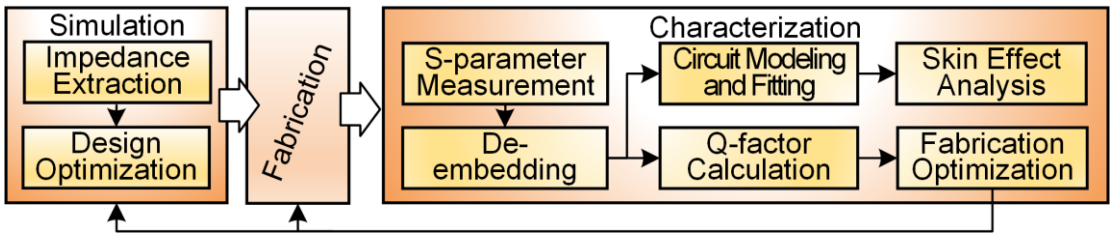


Figure 159: The flowchart of the study of MLG inductors.

First, based on the *impedance extraction* results, *design optimizations* for inductors are performed using simulations. Next, *fabrication* of test and de-embedding structures are performed. The *characterizations* are first performed by *S-parameter measurement,* followed by *de-embedding* procedures. By *circuit modeling and fitting*, the simplified circuit model is proposed and circuit parameters are extracted, based on which *skin effect analysis* is completed. On the other hand, using the de-embedded S-parameters, *Q-factor calculation* is performed, and subsequently *fabrication optimizations* (contact/dielectric effects) are carried out.

However, informative experimental studies on high frequency (HF) characteristics of graphene are rather sparse. Especially, the experimental study of practical graphene on-chip inductors have not been reported, neither have the design and fabrication optimizations. On the other hand, there is no experimental study and evidence of the skin effect (SE), an effect wherein HF current flow concentrates near the outer surfaces of conductors.

Therefore, in this section we perform the design, fabrication and characterization of graphene on-chip spiral inductors, as summarized in **Figure 159**. A circuit model is proposed and parameters are extracted from the fabricated inductors including ¾-, 2- and 3-turn inductors. For the first time, SE is investigated and is demonstrated to exist in each device. Fabrication optimization is also carried out to investigate the effects of isolation dielectric and contacts on the inductor performance. These results and findings provide necessary guidelines for future studies on graphene inductors as well as HF/RF applications of graphene and relevant 2D materials.

1. Design Optimization by Simulations

Q-factor of an inductor is an important metric in high-performance RF/mixed-signal circuits, which has to be optimized simultaneously w.r.t. its size (or design) and fabrication cost. To accomplish a superior design, it is very important to correctly understand the effect of each inductor parameter on the inductor performance.

Figure 160a,b show the schematic views (cross-section and stratified view) of a graphene on-chip spiral inductor structure, where the parasitics of the structure are marked. The series inductance (L_G) and resistance (R_G) of graphene are obtained by employing the impedance extraction procedure developed in **[59], [267]**. **Figure 160c** shows the equivalent circuit model proposed in this work, which is developed from conventional equivalent circuit for inductors **[61]**. The dimensions of the inductors are defined in **Figure 160d**. The simulation is performed for ¾-turn inductors since they have small area and low inductance values that are suitable for ultra-high frequency operation **[59], [267], [397]**.

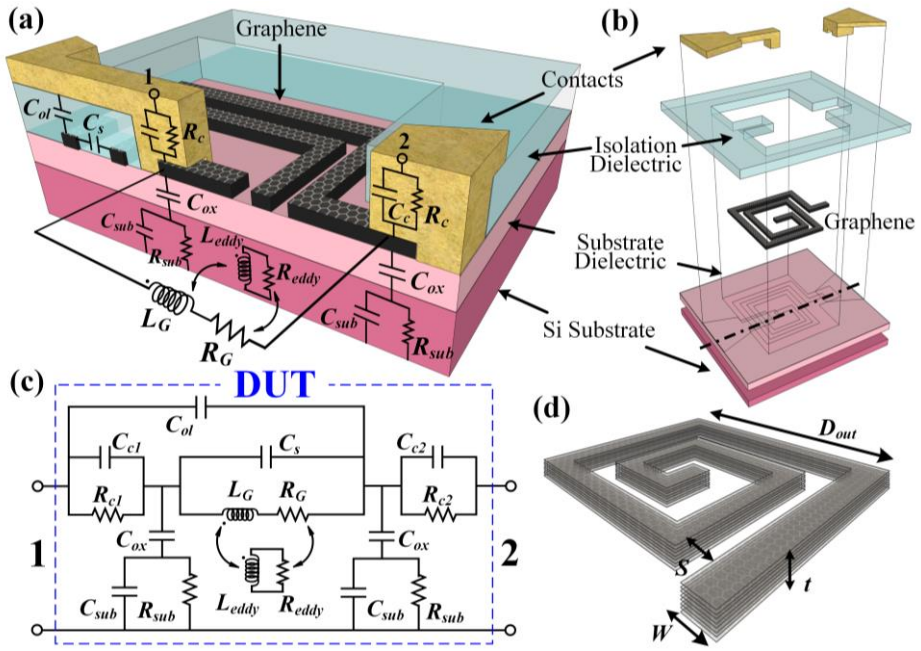


Figure 160: Schematic of graphene on-chip spiral inductor.

(a) Schematic view of graphene on-chip spiral inductor with the equivalent circuit parameters. L_G and R_G are the series inductance and resistance of graphene, respectively. C_s, C_{ol}, C_{ox}, C_{sub}, and R_{sub} represent the inter-turn coupling capacitance, overlap capacitance, substrate dielectric capacitance, substrate capacitance and resistance, respectively. R_c and C_c represent the contact resistance and capacitance, respectively. Eddy inductance and resistance, L_{eddy} and R_{eddy}, capture the eddy current effects in the substrate.

(b) Stratified view of (a). The dotted horizontal line indicates the plane where the cross-section in (a) is taken.

(c) Equivalent circuit model for the device under test (DUT) in (a), which is a two-port network.

(d) Schematic view of a graphene inductor coil, where D_{out}, W, t, and S are the outermost diameter, the conductor width, the conductor thickness, and the conductor spacing, respectively.

Figure 161 shows the effects of substrate resistance (R_{sub}), dielectric constant (ε_{ox}) and thickness (t_{ox}); and the total inductor length (L), inductor width (W), and inductor thickness (t) of graphene inductors on the Q-factor. It can be observed from **Figure 161a** that high Q-factor can be obtained by using low-loss (low-doping) substrate without shift of operation frequency (f_{op}) (the frequency at which the maximum Q-factor (Q_{max}) is achieved), due to the reduction of eddy current and energy loss. ε_{ox} and t_{ox} determine the dielectric capacitance C_{ox}, thereby affecting f_{op} and Q-factor, as shown in **Figure 161b** and **Figure 161c**. Q-factors first increase with L and W (**Figure 161d**, and **Figure 161e**) because of the increased inductance and reduced resistance, respectively, and then decrease with L and W due to the reduced magnetic coupling between the two ends and increased current proximity effect, respectively. However, as shown in **Figure 161f**, Q-factors increase with t due to increased number of conducting channels in graphene, which reduces the total resistance and energy loss. Hence, low-loss substrate, thick and low-permittivity substrate dielectric and thick graphene films should be chosen to obtain high Q-factors. W should be 2-4 μm, and L should be optimized to be as close to 400 μm as possible (albeit within the obtained graphene flake size).

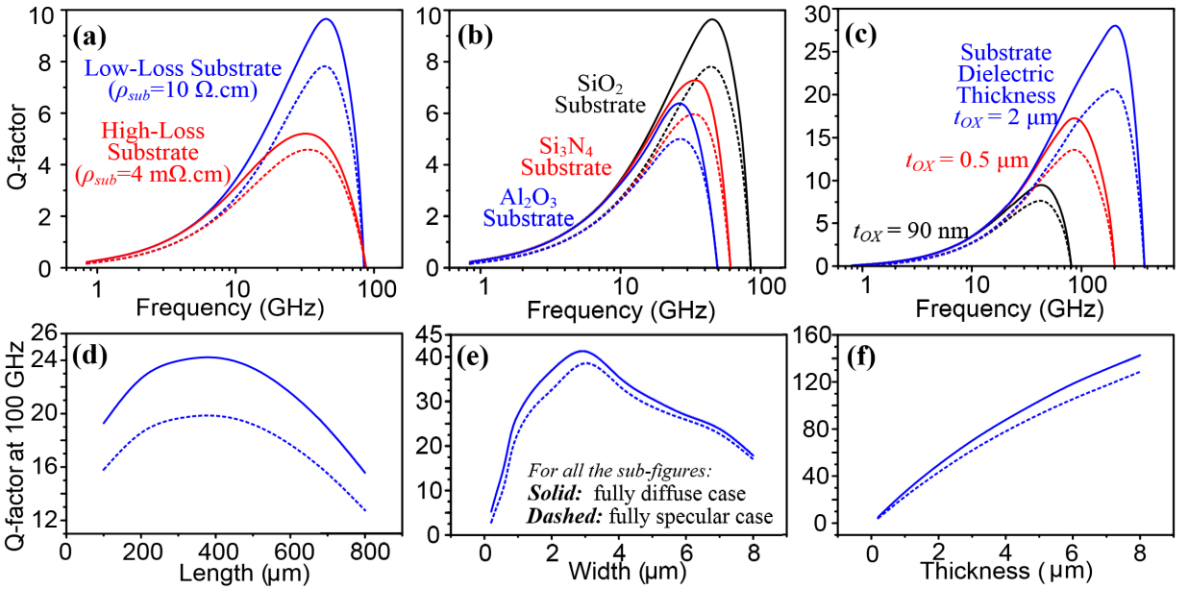


Figure 161: Design optimization of inductors by simulations.

The effects of (a) substrate resistivity, (b) substrate dielectric constant, (c) substrate dielectric thickness, (d) total inductor length, (e) inductor width, and (f) inductor thickness on the Q-factors of multilayer graphene-ribbon (GR) based ¾-turn inductors for ultrahigh frequency applications.

Two extreme cases of fully diffuse (solid curves) and fully specular (dashed curves) are considered in our simulation for each parameter. The substrate is chosen as 500-μm-thick silicon. The default total length (=3D_{out} for ¾- turn inductors), width, and thickness are 130 μm, 1 μm, and 1 μm, respectively. Low-loss substrate is used in (b-f). Substrate dielectric (SiO_2 in (a, c-f)) thicknesses are 90 nm for (a,b) and 0.5 μm for (d-f).

According to these results, low-loss substrate, thick and low-permittivity substrate dielectric and thick graphene films should be chosen to obtain high Q-factors. *W* should be 2-4 μm, and *L* should be as close as possible to 400 μm.

2. Fabrication of Graphene Inductors

Multilayer graphene films are prepared by mechanical exfoliation of highly ordered pyrolytic graphite (HOPG) and transferred onto SiO_2 (300 nm)/Si (10 Ω.cm) substrate. Subsequently, graphene films are patterned into ribbon coils. For multi-turn inductors, an isolation dielectric layer (Al_2O_3) over graphene is grown and patterned, the thickness (50 nm) of which is optimized to eliminate the effects of overlap capacitance (C_{ol}). Metal contacts and pads (Ni/Au: 20 nm / 80 nm) are deposited and patterned, followed by an annealing process. The entire fabrication process is illustrated by **Figure 162a-e**. **Figure 162f-i** show the micrographs and SEM images of some fabricated graphene inductors. The dimensions of all the devices are listed in **Table 12**.

Table 12: Graphene inductor sample information.

The sample labels, physical dimensions (D_{out}, W, t, and S), fitted circuit parameters (R_{G0}, L_{G0}, and C_s) using SE model, the SE model fitting coefficient (A), the maximum Q-factors (Q_{max}) and corresponding operation frequency (f_{op}) for all fabricated inductors. The first digit in the sample labels indicates the number of turns. It can be observed that f_{op} of the inductors are very high, especially for multi-turn inductors. This is because the inter-turn coupling capacitance, C_s, of these inductors is very small and cannot be appreciably increased due to the small thickness of graphene films.

Sample label	Dimensions				Fitted parameters				Q-factors	
	Dout (μm)	*W* (μm)	t (nm)	*S* (μm)	RG0 (Ω)	LG0 (nH)	Cs (fF)	A (THz-1)	fop (GHz)	Qmax
¾T-1	20	2	25	-	38.3	0.66	24.0	4.6	40.2	2.75
¾T-2	24	3	62	-	11.7	0.15	95.3	3.4	40.8	3.00
2T-1	50	3	64	3	20.4	0.27	26.3	1.4	53.3	2.80
2T-2	35	4	10	3	34.8	0.41	17.1	5.3	57.0	2.97
3T-1	40	2	30	2	30.7	0.33	21.6	2.9	57.0	3.52
3T-2	35	2	25	2	51.7	0.54	14.0	2.8	55.0	2.19

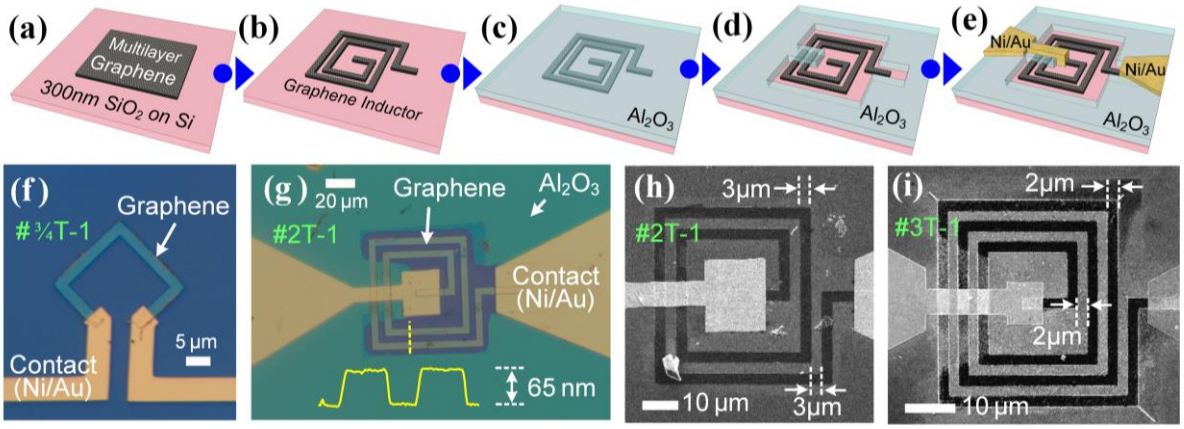


Figure 162: Fabrication processes of graphene on-chip inductor test structures.

(a) Preparation of graphene films on SiO_2 (300 nm) /Si (low-loss) substrate by mechanical exfoliation and thermal transfer; (b) Patterning of GR-based inductors by electron beam lithography; (c) Growth of 60 nm Al_2O_3 as isolation dielectric by atomic layer deposition at 150 °C; (d) Patterning of Al_2O_3 by KOH wet etching; (e) Deposition and patterning of metal contacts (Ni/Au: 20nm/80nm). (f, g) Optical photos of fabricated (f) ¾-turn and (g) 2-turn inductors. (h, i) SEM images of fabricated (h) 2-turn and (i) 3-turn inductors. The yellow curve in (g) shows the thickness profile measured by atomic force microscope along the yellow dashed line. The dimensions and labels of all the fabricated inductors are listed in Table I.

3. Measurement and De-embedding

The pad structures are designed as ground-signal-ground (GSG) coplanar waveguide (CPW) **[398]** with graphene test structure in the signal path. Subsequently, S-parameter measurements are performed in the frequency range of 100 MHz - 67 GHz using Agilent N 5227A Network Analyzer and a microwave probe station equipped with Cascade Infinity GSG-probes. As shown in **Figure 163**, to capture the intrinsic properties of the graphene

inductors themselves, de-embedding procedures **[398], [399]** are performed to stepwise remove the parasitic effects of the CPW using the dummy structures shown in **Figure 163a-d**.

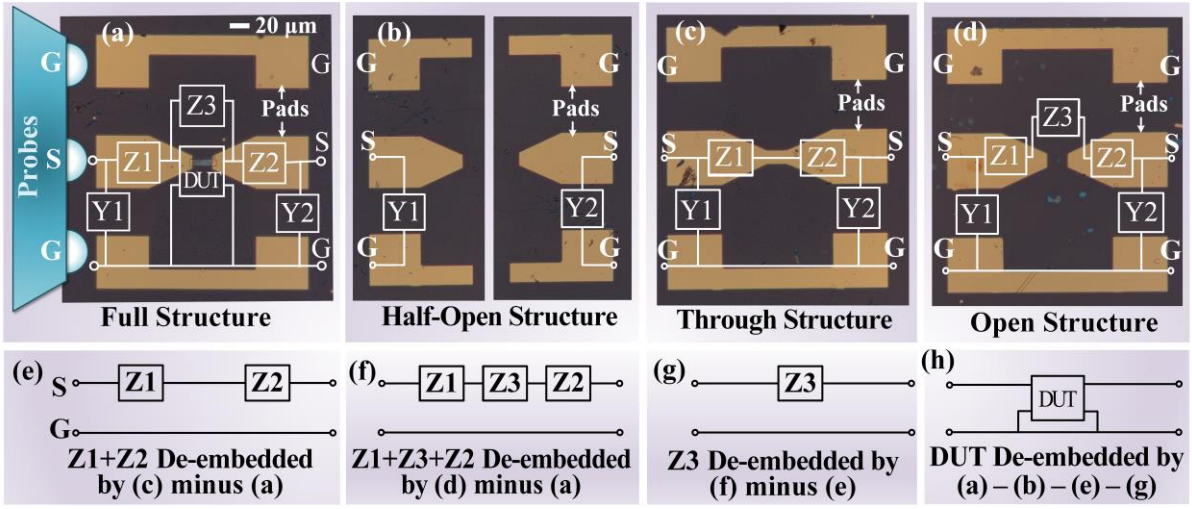


Figure 163: De-embedding procedures.

(a-d) optical photos of de-embedding structures and parasitic impedance circuit topology (white): (a) *full structure* (DUT with coplanar waveguide), (b) *half-open*, (c) *thru*, and (d) *open* structure. The *open* structure is identical to the *full structure* except that no DUT is in the gap of the signal conductors (S). The *half-open* structure is exactly half-cut of the *open* structure. The *thru* structure has continuous signal conductor. (e-h) The stepwise de-embedding procedure adopted in this work. Parallel parasitics Y_1 and Y_2 are obtained from the S-parameters of the *half-open*, and series parasitics Z_1 and Z_2 are extracted from the *thru* structure by removing Y_1 and Y_2. Series parasitic Z_3 is then de-embedded from the measured S-parameter of the *open* structure by removing Z_1, Z_2, Y_1, and Y_2. Finally the parameters of the DUT are extracted by stepwise removal of parasitics in (b), (e) and (g) from (a).

4. Circuit Model Fitting

As shown in **Figure 164a**, because the input impedance of the graphene device is smaller (larger) than that of the *open*/*half-open* (*thru*) structure, there are smaller (larger) signal reflection (S_{11}) and larger (smaller) transmission (S_{12}) in the graphene device.

In order to simplify the circuit model, the de-embedded S-parameter matrix (**Figure 164a,b**) of one test structure is converted to transmission (ABCD) matrix (**Figure 164c,d**). Since the ABCD matrix of all the fabricated samples possess the form of **(d)**, where A and D are equal to 1 and C is 0, **(e)** *the DUT* can be reasonably equivalent to **(f)** *the series impedance topology*. Hence, C_{ox}, C_{sub}, and R_{sub} can be neglected, for the low-loss low-C_{OX} substrate chosen and the frequency range. R_{eddy} and L_{eddy} are also neglected because of the frequency range. Besides, C_{ol} can be neglected because its effect does not affect the parameter fitting when isolation dielectric thickness is 50 nm. Moreover, the contacts are designed to be symmetrical, and therefore R_{c1}, R_{c2} and C_{c1}, C_{c2} can be simplified to R_c and C_c, respectively. Hence, the circuit model of DUT can be finally simplified to **(g)**.

Skin Effect (SE) investigation is carried out through fitting the circuit parameters to the measured data. As shown in **Figure 165**, large fitting error can be found in the fitted curve without considering skin effect (keeping R_G and L_G as constants over frequency), especially near low frequency, high frequency and the peak.

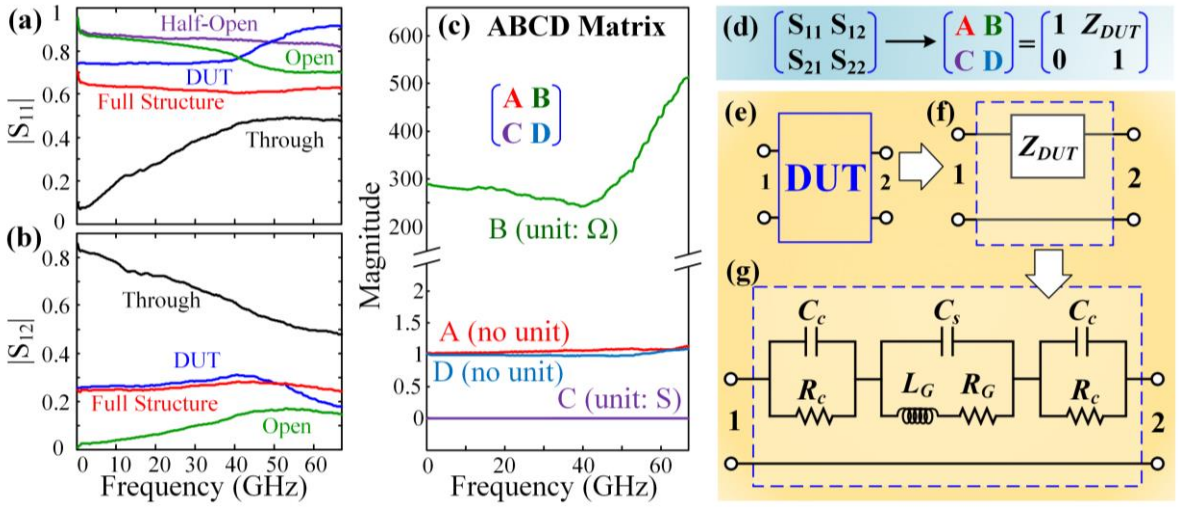


Figure 164: Simplification procedures of the equivalent circuit model.

Magnitude of (a) reflection (S_{11}) and (b) transmission (S_{12}) characteristics for *half-open*, *open*, *thru*, *full structure*, and *DUT* (taking device #2T-2 as an example). (c) Plots of the four elements of the transmission (ABCD) matrix, which is directly converted from the de-embedded S-parameters. (d) The conversion of S-parameter matrix to ABCD matrix. (e-g) Simplification procedures of the equivalent circuit model.

However, by modeling R_G and L_G as monotonical functions of frequency ($R_G(f)$ and $L_G(f)$), the circuit model can be perfectly fitted to the measured data. Several mathematic models (polynomials, square root, etc.) are utilized to model this SE, and the best fitting results are obtained from the exponential model, where $R_G(f)$ and $L_G(f)$ are modeled as exponential functions of frequency ($R_G(f) = R_{G0}\exp(\mathrm{A}f)$, $L_G(f) = L_{G0}\exp(-\mathrm{A}f)$, where A is a coefficient, and R_{G0} and L_{G0} are low frequency series resistance and inductance). The curves are different for different samples, indicating that A is varying among samples because of the different device dimensions.

This proves the existence of SE in graphene inductors, although having negligible SE is actually desirable. The resistance increases with frequency while the inductance decreases

with frequency for all the devices, which indicates SE exists in all of them.

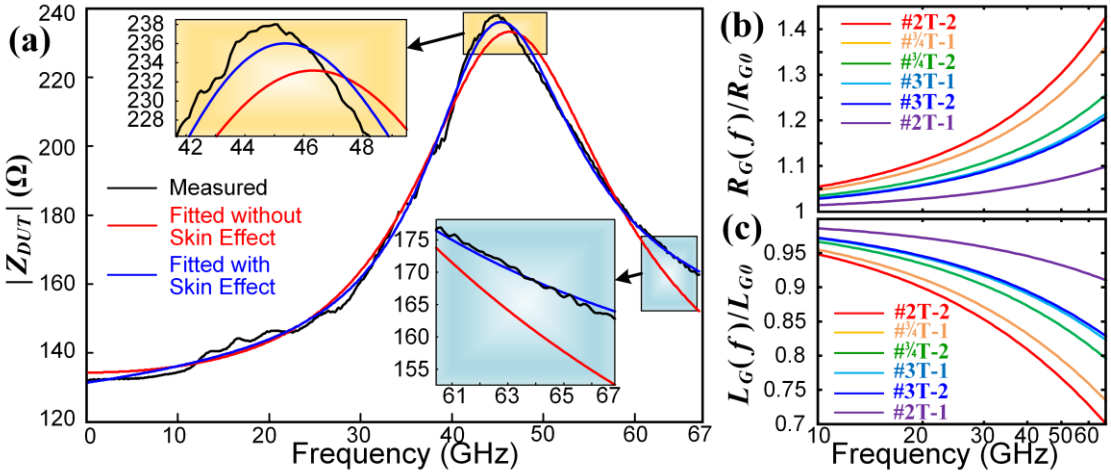


Figure 165: Fitting the circuit parameters to the measured data.

(a) The magnitude of DUT impedance (Z_{DUT}) as a function of frequency, including the measured data (inductor #¾T-2) and the fitted data using the circuit model in Fig.7g. Insets zoom into the peak and high frequency region. (b) Normalized resistance ($R_G(f)/R_{G0}$) and (c) normalized inductance ($L_G(f)/L_{G0}$) fitted from the measurement data of all the six fabricated devices.

5. *Q*-Factor Extraction and Fabrication Optimization

Q-factor is calculated by the equation Q = - imag(Y_{in})/real(Y_{in}), where Y_{in} is the input admittance at port 1 with port 2 shorted calculated from de-embedded S-parameters. All of the calculated maximum Q-factor (Q_{max}) and corresponding operation frequency (f_{op}) are shown in **Figure 166** and listed in **Table 12**. It can be observed that f_{op} of the inductors are very high, especially for multi-turn inductors. This is because the inter-turn coupling capacitance (C_s) of these inductors is very small and cannot be appreciably increased due to

the small thickness of the graphene films.

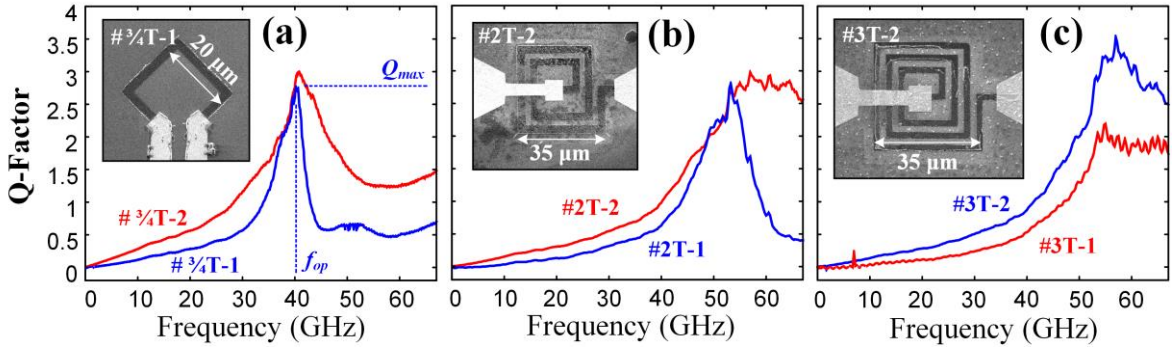


Figure 166: Q-factors vs. frequency of graphene inductors.

(a-c) the Q-factors vs. frequency of all the six fabricated devices: (a) ¾-turn inductors; (b) 2-turn inductors and (c) 3-turn inductors. Insets are example SEM images for the three types.

For multi-turn inductors, C_{ol}, and C_s are investigated and optimized by tuning the dielectric. The fabrication optimization is performed and illustrated in **Figure 167a-f**, on the same device. It can be observed in **Figure 167g** that C_s has significant influence on Q_{max}, and corresponding f_{op}, while C_{ol} only has capacitive influence on the Q-factor in the low-frequency range. C_{ol} becomes negligible when isolation dielectric thickness reaches 50 nm. Hence, Q_{max} and f_{op} can be optimized by dielectric engineering. **Figure 168** compares the Q-factors of inductor #3-1 before and after annealing. It can be clearly observed that the Q-factor increased by 2X after annealing, which is mainly due to the improvement of the quality of contacts (R_C reduced from 356 Ω to 318 Ω). Hence, contact engineering is also a necessity for further improvement of inductor Q-factors.

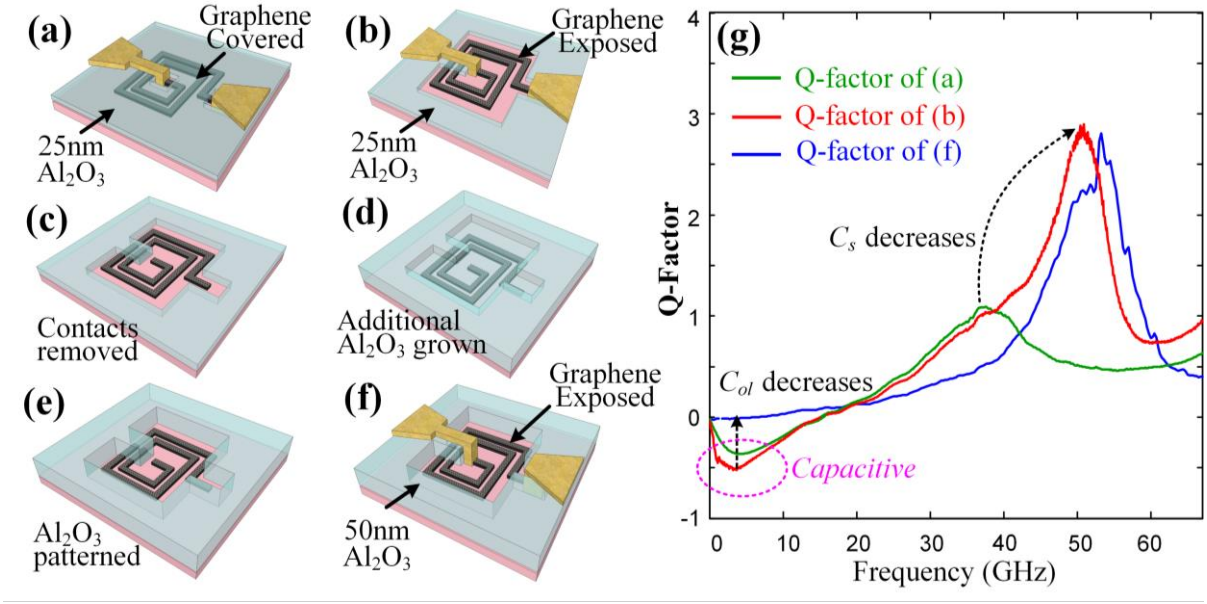


Figure 167: Fabrication optimization of MLG inductors.

(a-f) Schematics showing process flow of fabrication optimization of isolation dielectric on sample #2T-1: (a) device #2T-1 initially covered by 25-nm-thick Ai_2O_3 isolation dielectric; (b) device #2T-1 with coils exposed in air, where most area of the isolation dielectric in (a) is etched off; (c) #2T-1 with contacts removed by HCl; (d) #2T-1 with additional 25 nm Al_2O_3 grown; (e) #2T-1 with the 50-nm-thick Al_2O_3 patterned; (f) #2T-1 with new contacts deposited/patterned on the 50-nm-thick Al_2O_3. (g) The Q-factors of (a), (b), and (f) extracted after de-embedding.

As shown in **Figure 167g**, comparing (a) and (b), both Q_{max} and f_{op} increased, because after exposing the graphene coils in the air, the dielectric surrounding graphene is changed from high-k (Al_2O_3) to low-k (air) in (b), which decreases the inter-turn C_s. On the other hand, as shown in (g), the Q-factors of (a) and (b) are below zero in the low-frequency region, indicating the circuit is capacitive, which is due to the large C_{ol}. By increasing the thickness of the isolation dielectric, C_{ol} is decreased (in (f)), resulting in the returning of Q-

factor from capacitive to inductive in the low-frequency range. Q_{max} and f_{op} are hardly affected by C_{ol}. As discussed earlier, C_{ol} in the equivalent circuit can be neglected for 50 nm Al_2O_3. However, the circuit model in **Figure 160** cannot be fitted to devices with 25 nm Al_2O_3 isolation dielectric, indicating that C_{ol} cannot be neglected in that case.

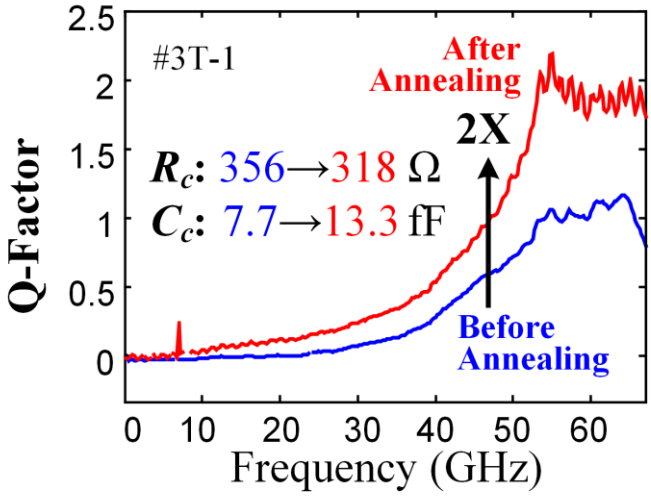


Figure 168: The Q-factors of inductor #3T-1 before and after annealing process.

Annealing process was performed at 400 K for 1 hour. It can be observed that by annealing process, the Q-factor is improved by 2X, which is mainly due to the improvement in the quality of metal contacts. The fitted R_c is changed from 356 Ω to 318 Ω, which serves as an evidence. The fitted C_c changes from 7.7 fF to 13.3 fF, one possible reason of which could be the improvement of interface adhesion and subsequent reduction in the gap between metal and graphene.

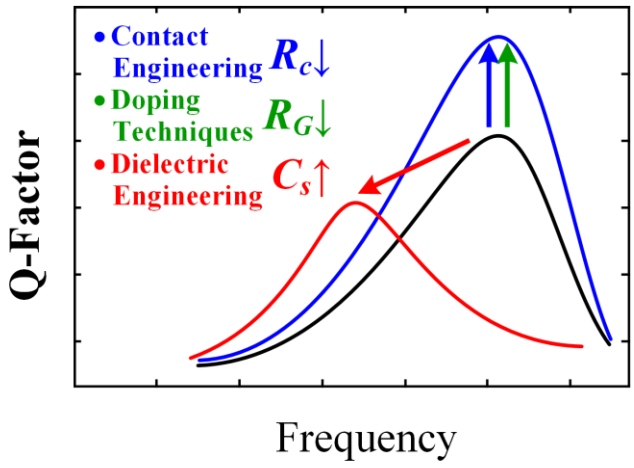


Figure 169: Strategies for improving of performance.

Q-factor sketch illustrating three strategies that can be adopted to improve the performance of graphene on-chip inductors. R_c and R_G can be reduced by contact engineering and proper doping techniques, respectively, thereby improving the Q-factor of inductors. Though the small thickness of graphene films results in low inter-turn coupling capacitances that make the f_{op}'s of the fabricated inductors in range of 40-60 GHz, C_s can be tuned by dielectric engineering and then f_{op} can be tuned to the desired frequency.

6. Summary of MLG Inductors

In this section, various graphene on-chip inductors are designed and fabricated. A circuit model is proposed and parameters are extracted by characterizing the fabricated inductors. Based on that, the existence of skin effect in multilayer graphene ribbons is experimentally demonstrated for the first time. This work also established pathways for design and fabrication optimizations of graphene on-chip inductors for the first time, providing guidelines for future inductor design as well as any high-frequency application based on

graphene, including the demonstration that the inductor performances (Q-factors and f_{op}) can be tuned by contact and dielectric engineering and doping techniques, aiming at different applications, as illustrated in **Figure 169**.

C. Intercalated MLG On Chip Inductors

1. Undoped MLG vs. Intercalated MLG

As shown in the previous section, there is a key challenge of using undoped MLG: the much lower conductivity of intrinsic MLG compared to conventional metals results in a significant performance loss, i.e., low (~ 3) *Q*-factors **[17]**. In addition, another severe challenge also exists, i.e., the interlayer coupling of MLG which reduces the charge carrier inertia and thus L_K.

To analyze the challenge of L_K drop, here we estimate the kinetic inductance of undoped MLG (or graphite) [1] and intercalated MLG (or graphite intercalation compound), compared with that of copper, since for small dimensions the kinetic inductance of carbon materials can be decades higher compared to magnetic inductances, due to their large momentum relaxation time **[61]**.

Although monolayer graphene has a linear *E*-*k* dispersion, in graphite or multilayer graphene, due to the strong interlayer coupling, the *E*-*k* dispersion is hyperbolic (Figure 123). Using the quadratic *E*-*k* approximation and hence the effective mass approximation, the kinetic inductance L_k per unit length of an *N*-layer MLG ribbon can be calculated in the

[1] It is worth noting that MLG and graphite are the same material in principle, because of the same lattice structure and stacking order, while graphite usually has more number of layers. However, giving the concrete number of layers to differentiate MLG and graphite is impossible. Since the technique demonstrated in this work applies both for MLG and graphite, we use the term MLG to represent both of the cases for the rest of the chapter.

Drude form as:

$$L_{k,MLG} = \frac{m^*_{MLG}}{n_{3D}e^2wt} = \frac{m^*_{MLG}}{n_{3D}e^2w\Delta t}\frac{1}{N} = \frac{m^*_{MLG}}{e^2w}\frac{1}{n_{2D}}\frac{1}{N} = \frac{L_{k0,MLG}}{N} \quad (36)$$

where $m^*_{MLG} = 0.043\ m_0$ is the effective mass of graphite **[400]**, n_{3D} is the volume carrier density, n_{2D} is the areal carrier density distributed in each layer, w is the ribbon width, t is the total thickness and $\Delta t = 0.34$ nm is the thickness of each layer. Here,

$$L_{k0,MLG} = \frac{m^*_{MLG}}{e^2w}\frac{1}{n_{2D}} \quad (37)$$

is the kinetic inductance contributed by each layer, which has $1/n_{2D}$ dependence. Hence, the total L_k decreases with the number of layers N, in the reciprocal form of $1/N$, which is exactly the parallel inductance formula.

However, by bringing the MLG layers farther from each other (i.e., by intercalation), the interlayer coupling can be alleviated and finally cancelled, if stage-1 intercalation is achieved. This is because the intercalation guest can effectively decouple the π–π interactions between adjacent graphene layers and expand the interlayer distance **[401], [402]**. Hence the *E*-*k* dispersion can be recovered from the hyperbolic form to the linear form (**Figure 123**) and thus $L_{k0,MLG}$ can be recovered to its monolayer value $L_{k0,1L}$.

Calculation of the kinetic inductance $L_{k0,GIC}$ for each decoupled layer in the intercalated MLG (or graphite intercalation compound, GIC) is still unclear. However, since decoupled graphene and monolayer graphene have the same linear *E*-*k* dispersion, we can attempt to estimate $L_{k0,GIC}$ for each decoupled layer in the way where the kinetic inductance of monolayer graphene is modeled **[403]**, using the effective collective mass per electron for monolayer:

$$m^*_{1L} = \frac{\hbar}{v_F}\sqrt{\pi n_{2D}} \quad (38)$$

where v_F is the Fermi velocity of graphene (~ 10^6 m/s) and $\hbar$ is the reduced Planck constant. By putting **Equation 37** into the Drude form of L_k, we can get:

$$L_{k0,\mathrm{GIC}} = \frac{m^*_{1\mathrm{L}}}{n_{2D}e^2w} = \frac{\sqrt{\pi}\hbar}{v_F e^2 w}\frac{1}{\sqrt{n_{2D}}} \tag{39}$$

It is worth noting that $L_{k0,\mathrm{GIC}}$ has a $1/\sqrt{n_{2D}}$ dependence instead of $1/n_{2D}$, and typically $L_{k0,\mathrm{GIC}} > L_{k0,\mathrm{MIG}}$ can be found for most practical $n_{2\mathrm{D}}$ values.

Hence, the kinetic inductance of stage-1 intercalated MLG is:

$$L_{k,\mathrm{GIC}} = \frac{L_{k0,\mathrm{GIC}}}{N} = \frac{\sqrt{\pi}\hbar}{v_F e^2 w}\frac{1}{\sqrt{n_{2D}}}\frac{1}{N} \tag{40}$$

It is also worth noting that for carbon nanotube (CNT) bundles, even without intercalation, the inter-tube coupling/interaction can be ignored, and hence the kinetic inductance of each conducting channel in the bundle, $L_{k0,\mathrm{CNT}}$, is exactly the same as in a single CNT **[61]**. Hence, The total kinetic inductance of a CNT bundle scales as $L_{k,CNT\ bundle} = L_{k0,\mathrm{CNT}} / N$, similar to equation S12.

For GIC stage number greater than 1, for example, stage-3, the energy dispersion is a combination of hyperbolic and linear forms, very similar to a trilayer graphene, as shown in **Figure 123**. Hence, the kinetic inductance of each 3 layers can be considered as the parallel inductance of both the hyperbolic modes and the linear modes, as $L_{k0} = (\Sigma\ L_{k0,\mathrm{MLG}}^{-1} + \Sigma\ L_{k0,\mathrm{GIC}}^{-1})^{-1}$. Note that m^*_{MLG} of trilayer graphene in $L_{k0,\mathrm{MLG}}$ is slightly different from that of MLG **[400]**.

For comparison, the kinetic inductance per unit length of copper is

$$L_{k,\mathrm{Cu}} = \frac{m^*_{Cu}}{n_{3D}e^2wt} \tag{41}$$

where the electron effective mass of copper is taken as $m^*_{\mathrm{Cu}} = 1.01\ m_0$ **[404]** and the electron density of copper is $n_{3\mathrm{D}} = 8.49 \times 10^{28}$ m^{-3}. Note that this calculation is valid for bulk Cu only

(hundreds of nm thick), since the size effect can significantly impact the effective mass and carrier density when Cu is scaled to sub-100 nm dimensions.

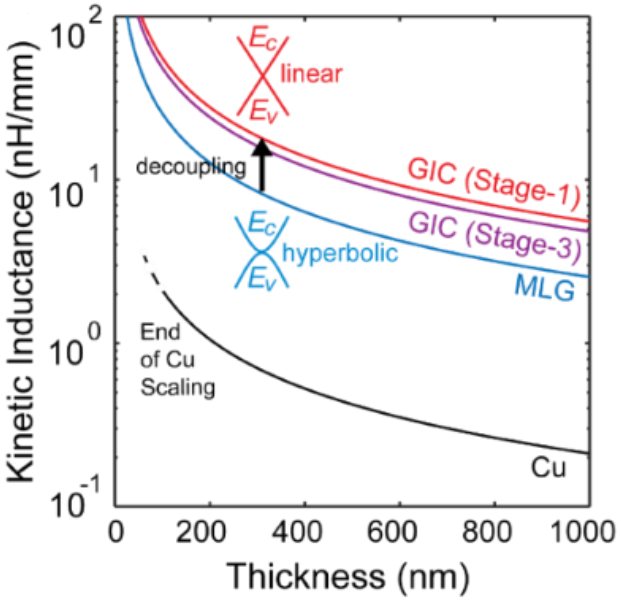


Figure 170: Comparison of kinetic inductances.

Kinetic inductances (L_k) per unit length *vs*. thickness of MLG, graphite intercalation compound (GIC) and Cu are shown. The ribbon widths are all 2 um. The equivalent volume carrier density in MLG and GIC is 3×10^{20} cm^{-3}, and 8.49×10^{22} cm^{-3} in Cu. Insets illustrate the band structures of MLG and GIC.

As shown in **Figure 170**, the L_k's of MLG, stage-3 GIC and stage-1 GIC, as well as Cu are plotted and compared. It can be seen that graphene in the form of both MLG and GICs has much higher L_k than that of Cu. It can also be seen that the intercalation doping can improve L_k from the blue curve (MLG) to the purple curve (stage-3 GIC) and finally the red curve (stage-1 GIC), due to the interlayer decoupling effect. In **Figure 170**, w = 2 μm is assumed for MLG, GICs, and Cu; the same equivalent volume carrier density $n_{3D} = 3\times10^{20}$

cm^{-3} **[57]** is assumed for MLG, stage-3 and stage-1 GICs ($n_{2D} = n_{3D} \times t_i$, where t_i is defined in **Figure 124**).

It is worth noting that although using MLG actually reduces the L_K compared to monolayer graphene, we still must have MLG since MLG ensures that the contact resistance is lowered to acceptable value.

2. Proposed Solution

It can be seen that the intercalation doping can improve L_k by the interlayer decoupling effect. Here, an unique on-chip inductor based on intercalated MLG is demonstrated (**Figure 171a**). We will show that without performance loss, the technique has overcome the fundamental scalability challenge in conventional inductors, by exploiting the high kinetic inductance and high conductivity of intercalated MLG. Specifically, bromine (Br) intercalation is employed to demonstrate such technique (**Figure 171c**), which boosts both MLG conductivity (by increasing the carrier density via doping effect), and L_K by interlayer decoupling (**Figure 171d**). The technique leads to sufficiently high *Q*-factors up to 12 in a typical two-turn layout, and up to 1.5x higher inductance density w.r.t Cu counterparts with the same layout and *Q*-factors, which translates to an area reduction of about one-third. Such high performance and area efficient spiral intercalated MLG inductors inherently provide unprecedented scalability, design flexibility and discreetness for next-generation RF-ICs and RF-ID technology needed to realize the IoT paradigm. Moreover, intercalated MLG has been recently demonstrated to address the fundamental current-carrying capacity problem of scaled Cu interconnects used in IC applications **[15]**. Hence, our demonstration of intercalated MLG inductors could provide an “all-graphene” back-end-of-line (BEOL) conductor technology for next-generation ICs to provide the ultimate performance and reliability in possibly smallest form factor.

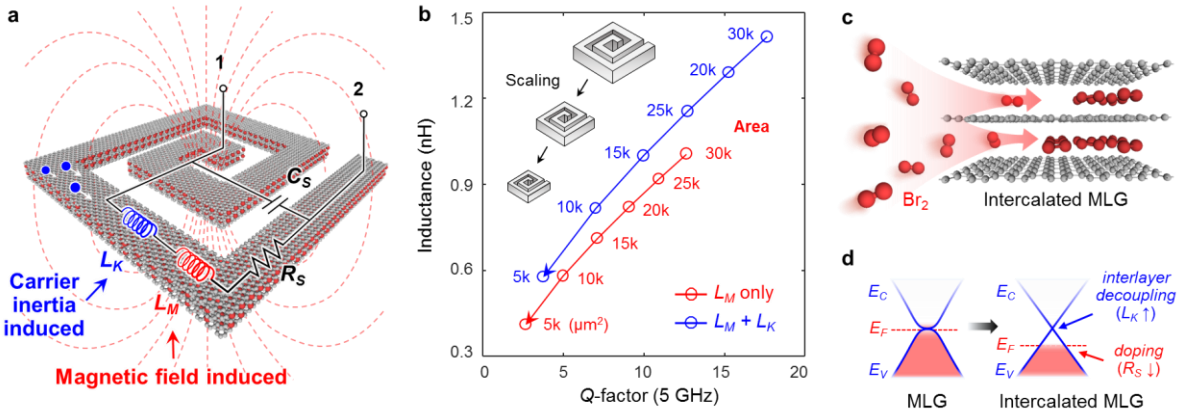


Figure 171: Concept of intercalated MLG on-chip inductors.

(a) Schematic of a spiral inductor and its simplified equivalent circuit (two-port network). L_M and L_K represent the magnetic and the kinetic inductances, respectively. Red dotted curves represent the time-varying magnetic field, which results in L_M (both self and mutual). Blue dots represent the charge carriers with inertia, which results in L_K. R_S and C_S represent the series resistance and the inter-turn capacitance, respectively. The substrate and its parasitics are not shown. (b) Simulated total inductance and *Q*-factor (at 5 GHz) of a 2-turn inductor with area (= outer diameter^2) scaling, for conventional Cu inductors without L_K (red) and with artificially added L_K (blue). Each parameter other than L_K is assumed to be identical for both cases. In the case with L_K, L_K is assumed to be 50% of the value of L_M, which is proven to be experimentally achievable by intercalated MLG later in this work. The corresponding area is marked next to each data point. Insets illustrate how the layout is scaled. See Supplementary Material Section 4 for more details about (a) and (b). (c) Schematic of the bromine (Br_2) intercalated MLG used as the spiral material in this work. (d) Effects of intercalation on the band structure: shift of Fermi level by doping effect and change of shape (hyperbolic to linear) by interlayer decoupling effect.

3. Fabrication of Intercalated MLG

As the proposed material to form the spiral structure in **Figure 171a**, intercalated MLG is first prepared. As discussed in **Chapter V**, among all those intercalation guest options, Br intercalation is interesting due to its simple process and high efficiency.

To realize the Br intercalation, millimeter-sized highly oriented pyrolytic graphite (HOPG) slices were first transferred onto quartz (SiO_2) substrates (1 cm × 1 cm × 1 mm) at room temperature and then set in a glass tube. After evacuation down to 0.5 Pa, the samples were exposed to Br_2 gas at room temperature for 90 minutes using a two-zone vapor transport method.

Since Br_2 easily diffuses deeply into graphite, the doping process can be performed on both large MLG flakes and MLG ribbons. It is worth comparing the doping effects for these two scenarios. Hence, as shown in **Figure 172**, the samples have been divided into three groups – *pristine* (undoped), *doped-after-etching* (doping was performed after MLGs were patterned into ribbons) and *doped-before-etching* (doping was performed before MLG flakes were patterned) for comparison. Note that the samples referred in the main text are all *doped-before-etching* samples due to their eventual better results.

To fabricate the samples, millimeter-sized HOPG slices were first transferred onto isolating substrates. For four-probe samples, both SiO_2 (330 nm)/Si (10 Ω.cm) substrates and quartz substrates were tested and it turns out that the substrates do not affect the subsequent characterization steps such as atomic force microscopy and four-probe DC measurements. For inductor samples, only quartz substrates were used due to lower substrate loss. The MLG flakes were patterned into ribbons using oxygen inductive coupled plasma, the etching rate of which is more than 100:1 for MLG:SiO_2. In this work, doped MLG ribbons with widths in the μm range are of interest, since such sizes are more suitable

for on-chip inductors widely employed in super high-frequency (SHF) hardware working below 40 GHz including wireless internet, wireless USB, cell phones, and some radars and satellites. Hence, the ribbon width is varied among 4/6/8/12/16 (for four-probe measurements) and 20/25 μm (for inductor spirals) and thickness is varied in the 50 – 2000 nm range. Metal contacts and pads (Ni/Au: 40 nm / 760 nm) were deposited and patterned with four terminals in order to perform four probe measurements.

For Br intercalation, the samples were set in a glass tube. After evacuation down to 0.5 Pa, the samples were exposed to Br gas at room temperature for 90 min using a two-zone vapor transport method **[337]**. It is worth noting that Br intercalation process is corrosive, and can remove any metal contacts that are exposed to Br. Hence, metal deposition has to be performed after intercalation.

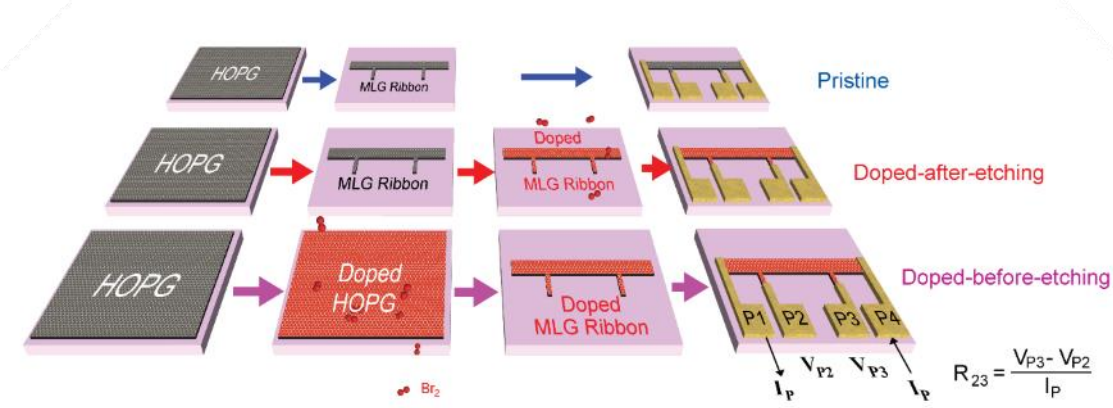


Figure 172: Fabrication process flows of MLG ribbons.

MLG ribbons include pristine, doped-after-etching, and doped-before-etching samples for four-probe measurements.

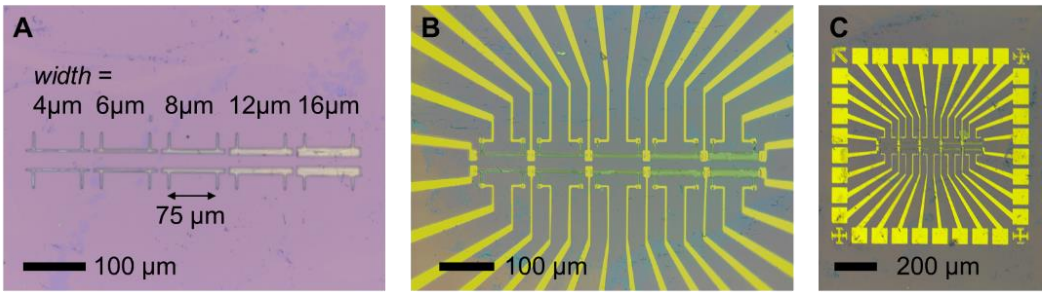


Figure 173: Microscope photos of MLG ribbons for four-probe measurements. (A) Samples before depositing metal contacts; (B, C) Samples after depositing metal contacts.

4. Characterization of Intercalated MLG

AFM measurements were performed on both the pristine and the doped samples to measure the ribbon thicknesses. To minimize the random error of thickness measurement, for each sample, instead of a single scan route, a height distribution plot was generated from a height profile measured over 100 μm^2 area containing both ribbon and substrate (**Figure 174A,B**). Subsequently, the thickness was taken as the difference between the two height distribution peaks (**Figure 174C**). A few samples were measured both before and after doping. The thickness increment averaged from these samples is around 6.7% of their original thicknesses (**Figure 174D**), which is in agreement with our previous results on bulk HOPG **[337]**.

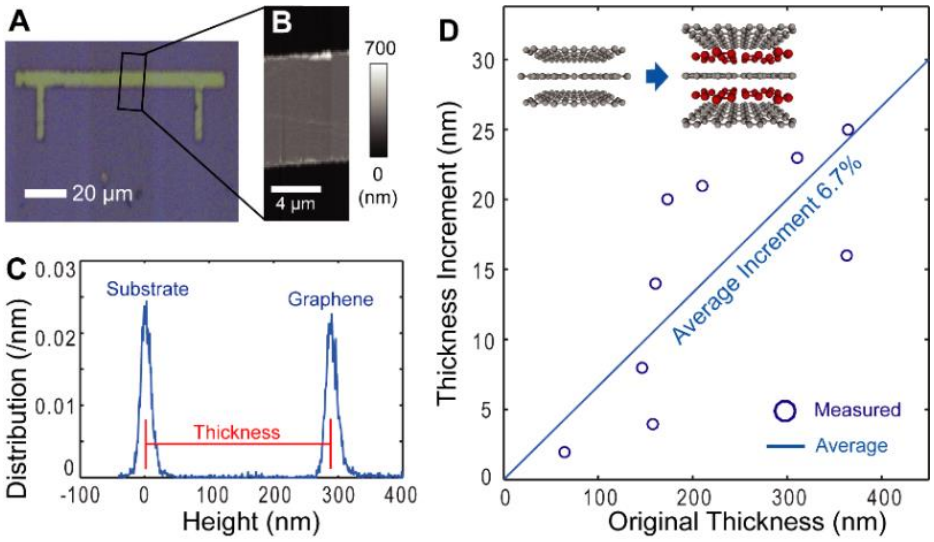


Figure 174: AFM measurements of intercalated MLG

(A) Microscopic photo of a MLG ribbon for AFM measurement. (B) AFM height profile of the black rectangle in (A). (C) Height distribution of the profile in (B). (D) Thickness increment after doping for MLG ribbons with various initial thicknesses.

The cross-section view images of the intercalated samples generated by STEM are shown in **Figure 175A** and **B** (zoomed), where dark layers and light layers are alternately stacked, indicating mixed stack. To further investigate the composition of the mixture, EDX measurement was performed. **Figure 175C** shows an EDX mapping of Bromine's K-shell characteristic X-ray signal, where purple indicates high Br concentration detected, while **Figure 175D** shows carbon's K-shell signal, where darker signals indicate lower C concentration in the GIC regions. It is clear from **Figure 175** that the majority of bromine is intercalated to random regions of graphene layers, leaving other regions lightly doped. Hence, the doped sample is a stacked mixture of highly doped MLG and low doped MLG.

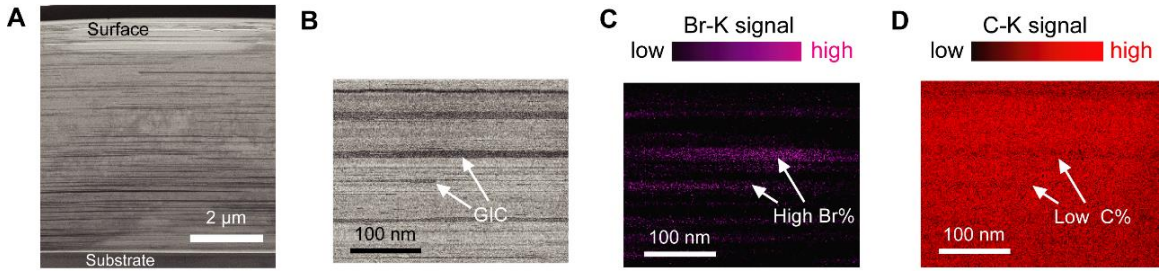


Figure 175: STEM and EDX characterization of of intercalated MLG

(A, B) STEM images of the cross section of a doped flake showing the mixed stack of GIC and MLG. (C, D) EDX images of (C) Bromine-K signal and (D) Carbon-K signal, wherein the GIC regions with high bromine signal and low carbon signal are observed, respectively.

The Br concentration was measured by XPS and the work function was measure by UPS in the same analysis tool using different excitation sources. The average concentration of Br atoms is about 3%, according to the XPS measurements on 9 spots from 3 different wafers (**Figure 176**). There is no clear dependence of work function (WF) on Br concentration, as shown by UPS results. One possible reason why the WF varies, is because the UPS measurements are sensitive to the surface condition such as roughness and impurities.

Raman spectroscopy confirmed the existence of intercalation (due to new Br-peak and GIC-peak, as well as shift of G-peak) and a GIC stage number (= # of graphene layers over # of intercalation layers) of about 3 in the highly doped region.

For the *doped-before-etching* samples, 532 nm laser was used, and no background fluorescence was observed. For the *doped-after-etching* samples, 532 nm laser was firstly used. However, strong background fluorescence was observed, which may have come from residue during patterning process. Subsequently, 633 nm was used for *doped-after-etching* samples due to a lower fluorescence.

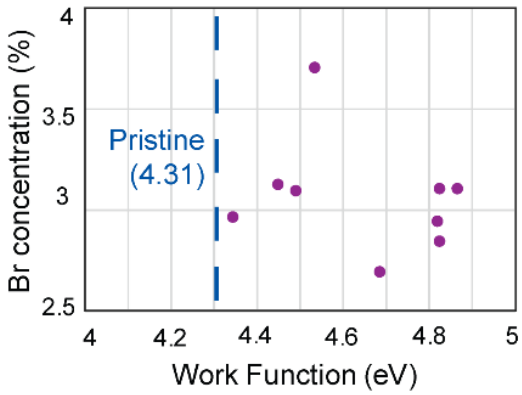


Figure 176: XPS and UPS characterization of intercalated MLG

XPS/UPS measurement results on 9 spots on 3 wafers with doped MLG. The increase in WF after intercalation confirms p-type doping.

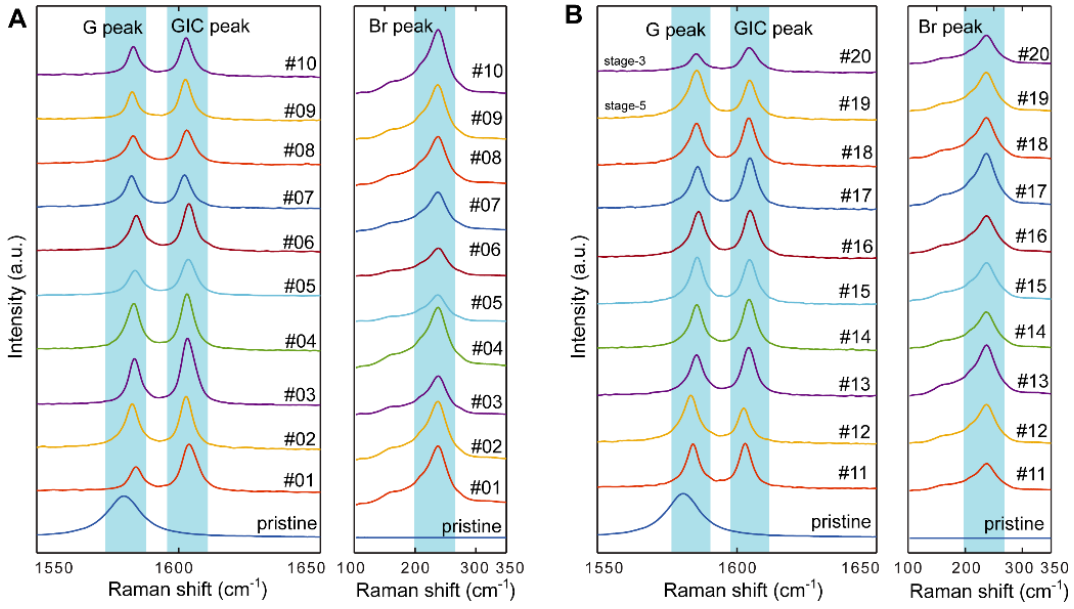


Figure 177: Raman spectra of intercalated MLG.

(a) Raman spectra of 10 *doped-before-etching* samples with thicknesses of about 5 − 10 µm. (b) Raman spectra of 10 *doped-before-etching* samples with thicknesses of few µm. All spectra are measured with 532 nm laser.

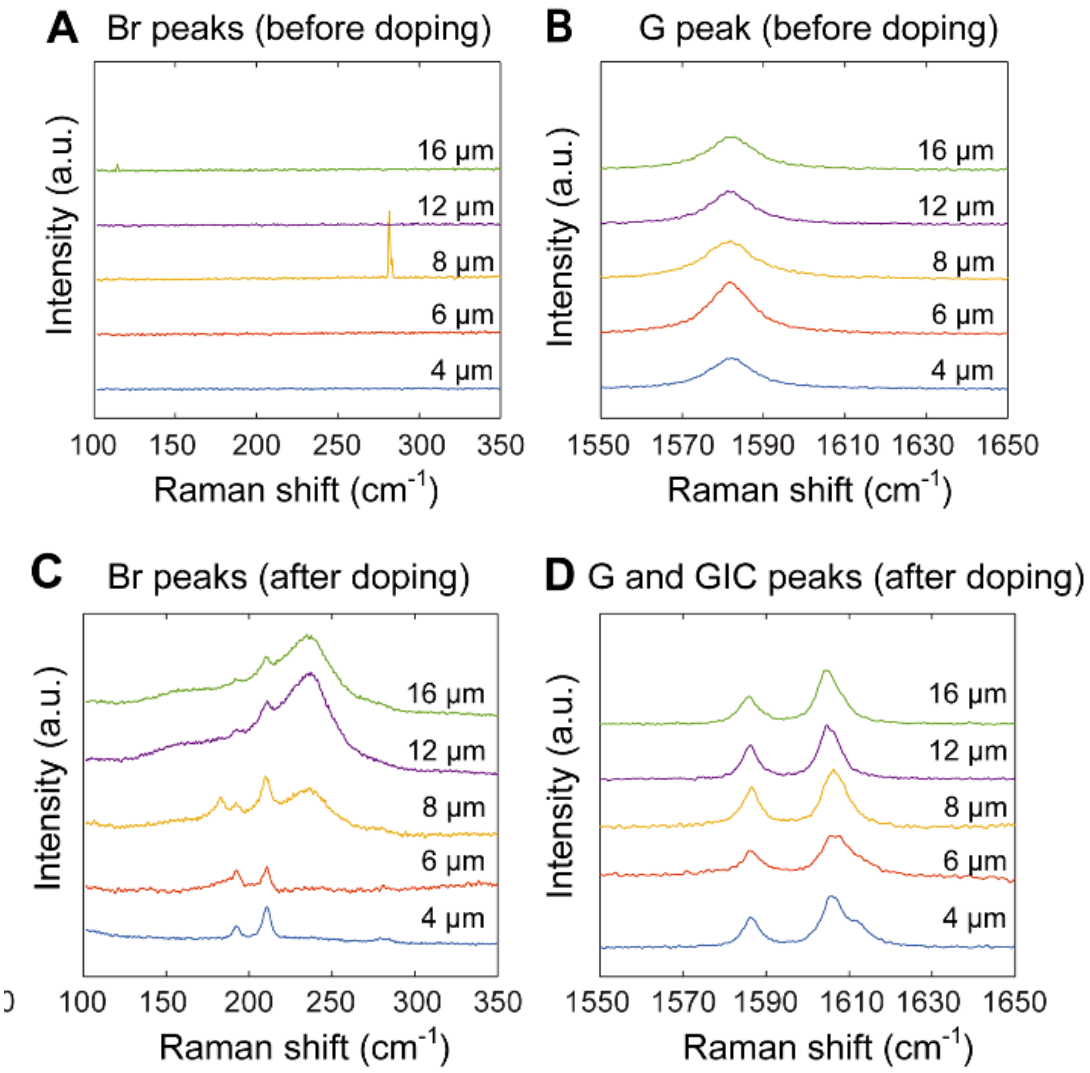


Figure 178: Raman spectra of intercalated MLG.

Raman spectra for a group of 5 *doped-after-etching* samples with different widths (4, 6, 8, 12 and 16 μm, from bottom to top) show (A) Br peak before doping; (B) G peak before doping; (C) Br peak after doping and (D) G and GIC peaks after doping. All spectra are measured with 633 nm laser.

Almost all of the GIC/G peak ratios of the samples are > 1, indicating the evidence of the intercalation doping, as shown in **Figure 177**, **Figure 178** and **Figure 179**. It is considered that the intercalation stage number of the Br-doped MLG was estimated to be 3 −

5 (stage-3 for most of the data) by comparing the shape of the Raman spectrum and the peak shifts in the G and GIC peaks with those reported in Ref. **[333]** (in **Figure 180**).

For *doped-after-etching* samples, there is no clear dependency of the GIC/G ratio (= GIC_{max} (1600~1610 cm^{-1}) / G_{max} (1580~1590 cm^{-1})) on the width, as shown in **Table 13**.

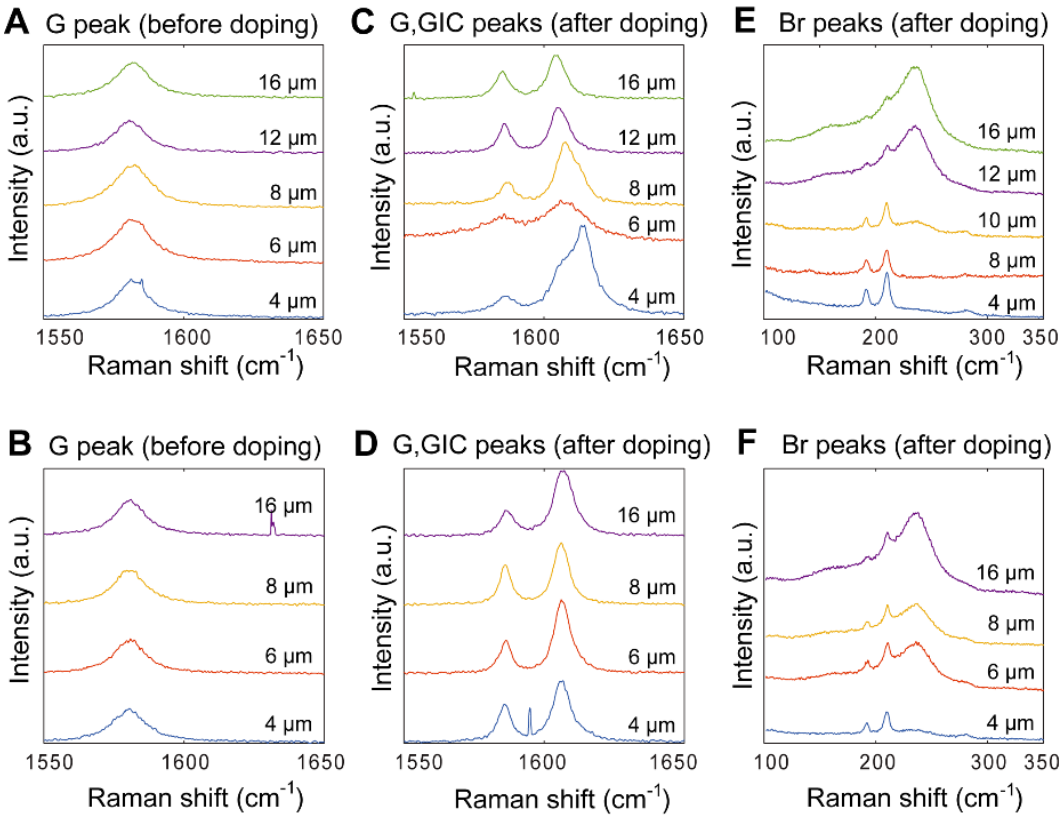


Figure 179: Raman spectra of intercalated MLG.

Raman spectra for two other groups of *doped-after-etching* samples with different widths show (A, B) G peak before doping; (C, D) Br peak after doping and (E, F) G and GIC peaks after doping. All spectra are measured with 633 nm laser.

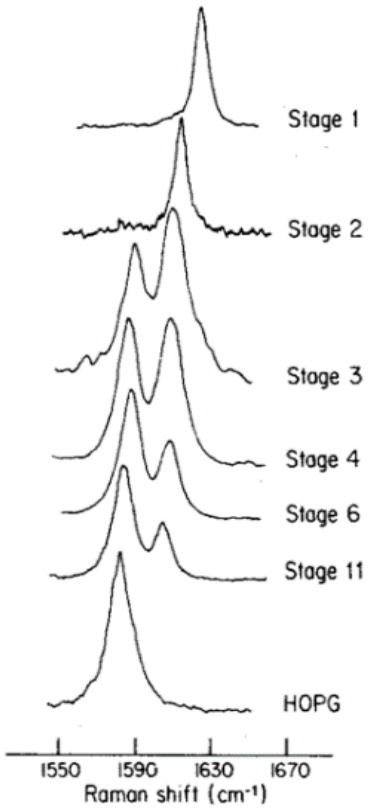


Figure 180: Raman spectra of intercalated MLG with different intercalation stages. Adopted from Ref. [333] with permissions from *Taylor & Francis*.

Table 13: Peak positions and ratios measured from a group of *doped-after-etching* ribbons. All spectra are measured with 633 nm laser.

	G-peak before doping (cm^{-1})	G-peak after doping (cm^{-1})	GIC-peak after doping (cm^{-1})
w = 4 μm	1582.5	1586	1604
w = 6 μm	1582	1586	1606
w = 8 μm	1582.5	1587	1607
w = 12 μm	1581	1586	1605
w = 16 μm	1582	1585	1604.5
Stage-3 (Ref. **[333]**)	N/A	1587	1608

6 HOPG samples with size of 7 mm × 7 mm were prepared. 3 of them were doped by Br. The flake thicknesses were measured by laser microscope at 3 points per sample.

Then, Hall measurement was carried out using Van Der Pauw method. Each HOPG flake was contacted with 4 terminals (*a*, *b*, *c*, *d*) using Ag paste, and the measurement was performed under a magnetic field of 0.765 T at 295 K. The thickness, resistivity, sheet resistance, Hall coefficient, carrier density, carrier mobility and carrier type of each sample were obtained and listed in **Table 14**. It can be seen that the conductivity obtained by Hall measurement can be improved by ~5X by Br doping, and the carrier density can be improved by approximately one decade, although a degradation (from ~5X to ~3X) after patterning into ribbons is observed, as discussed later. In addition, there is no significant change in the carrier mobility, possibly due to the fact that the improvement from energy dispersion change and the negative effect of impurity scattering cancel each other out. The formulas used for the calculations are:

$$\begin{cases} \textbf{Resistivity (Ω·cm):}\ \rho = (\pi t)/ln2 \times R_{ab,cd} f\ \textbf{;} \\ \textbf{Sheet resistance (Ω):}\ R_{sheet} = \pi/ln2 \times R_{ab,cd} f = \rho/t\ \textbf{;} \\ \textbf{Hall coefficient (cm}^{\textbf{3}}\textbf{/C):}\ R_H = t/B \times V_{HALL}/I_s\ \textbf{;} \\ \textbf{Carrier density (cm}^{\textbf{-3}}\textbf{):}\ n = 1/(R_H e)\ \textbf{;} \\ \textbf{Mobility (cm}^{\textbf{2}}\textbf{/V·s):}\ \mu = R_H/\rho\ \textbf{.} \end{cases} \quad \textbf{(S14)}$$

In these equations, $R_{ab,cd}$ equals V_{dc}/I_{ab}, voltage measured at *c* and *d* over current measured between *a* and *b* , where *a*, *b*, *c*, *d* are the four terminals clockwise; *f* is a factor that is a function of $R_{ab,cd}/R_{bc,da}$; *B* is the magnetic field; V_{HALL} is the Hall voltage measured from two diagonal terminals; I_s is the current measured from the other two diagonal terminals; and *t* is the flake thickness.

Table 14: Hall measurement results.

The thickness, resistivity, sheet resistance, Hall coefficient, carrier density, carrier mobility and carrier type of undoped samples (HOPG) and doped samples (Br-GIC).

Sample	Thickness *t* [μ m]	Resistivity ρ [Ω · cm]	Electrical conductivity σ = 1/ ρ [S/cm^{-1}]	Sheet resistance R_{sheet} [Ω/□]	Hall coefficient R_H [cm^3/C]	Carrier density n [cm^{-3}]	Mobility μ [cm^2/Vs]	Carrier type
HOPG 1	2.80	8.35×10-5	1.20×10^{4}	2.98×10^{-1}	-1.61×10^{-2}	3.89×10^{20}	1.93×10^{2}	n-type
HOPG 2	7.47	7.28×10-5	1.37×10^{4}	9.75×10^{-2}	-6.28×10^{-2}	9.93×10^{19}	8.62×10^{2}	n-type
HOPG 3	2.03	5.64×10-5	1.77×10^{4}	2.78×10^{-1}	-3.70×10^{-2}	1.68×10^{20}	6.56×10^{2}	n-type
Br-GIC 1	2.94	1.20×10-6	8.31×10^{4}	4.09×10^{-2}	5.89×10^{-3}	1.06×10^{21}	4.89×10^{2}	p-type
Br-GIC 2	1.83	1.17×10-6	8.52×10^{4}	6.40×10^{-2}	8.90×10^{-3}	7.01×10^{20}	7.59×10^{2}	p-type
Br-GIC 3	2.57	1.04×10-6	9.63×10^{4}	4.04×10^{-2}	4.31×10^{-3}	1.45×10^{21}	4.15×10^{2}	p-type

Four-Probe Measurements show that the average conductivity (median of the fitting curve based on normal distribution) of all the 51 *doped-after-etching* ribbons is 4.3 S/μm (**Figure 181** center), which is 2.4X that of pristine MLG (HOPG) (**Figure 181** top) and one decade higher than that of bulk graphite. The average conductivity of all the 53 *doped-before-etching* samples is 5.1 S/μm (**Figure 181** bottom), which is even better (2.83X). However, these 53 samples exhibit more variation and thus larger standard deviation (σ = 3.3), indicating that the distribution of dopants induced by the *doped-before-etching* method is less uniform. According to our previous characterizations **[337]**, the Br concentration was found to be higher at the surface and gradually decreased inside the film. This is the nature of any diffusion process. Hence, the non-uniform thickness of the exfoliated HOPG samples can result in such non-uniformity in the doping. The non-uniformity can be resolved using CVD samples in which there is less thickness variation.

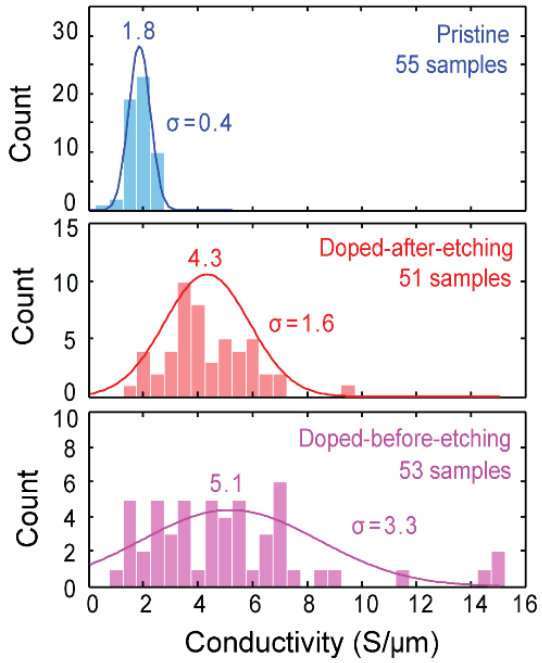


Figure 181: Four-probe measurement results.

Distribution plots of the conductivity measured from all the MLG ribbons. Bars represent sample counts, while curves represent fitting results based on normal distribution.

It is interesting that there is a clear but different dependence of the conductivity on the ribbon width for the two doped groups. As shown in **Figure 182**, *doped-before-etching* samples have better conductivity for larger widths. This is because it is easier for bromine to diffuse out from narrower ribbons. For *doped-after-etching* samples, since the ribbon edges may get fused by high power oxygen plasma, it is more difficult for bromine to diffuse into wider ribbons deeply. Hence, conductivity of 12 and 16 μm wide doped-after-etching ribbons decreases. In brief, for ribbons narrower than 10 μm, *doped-after-etching* method is suggested, while for ribbons wider than 10 μm, *doped-before-etching* method is suggested due to better doping efficiency and up to 3.2X higher conductivity can be achieved on 16-

μm-width *doped-before-etching* ribbons, compared to pristine MLG.

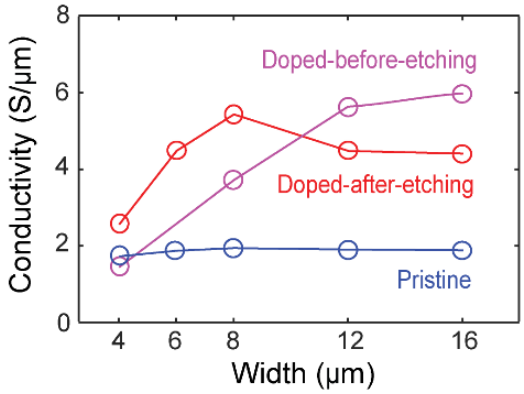


Figure 182: Conductivity vs. ribbon width.

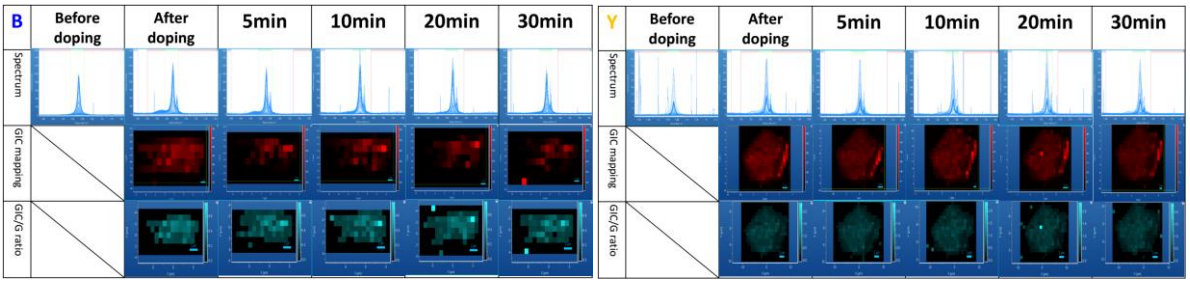
Comparison plot of conductivity vs. ribbon width for the three sample groups, where different width dependencies can be observed for the three groups.

The stability of Br intercalated MLG was firstly evaluated by dipping into acetone, isopropanol alcohol (IPA), and ethanol (**Figure 183**), which are the chemicals widely used in semiconductor processing. Br-intercalated MLG flakes were transferred onto three SiO_2/Si substrates. Each wafer includes 2 flakes with thickness of several 10 nm, and 2 additional flakes with thickness of several 100 nm. They were dipped in acetone, IPA, and ethanol separately for 5, 10, 20 and 30 min. The Raman spectra were compared before and after the dipping. There were no clear differences in the GIC/G ratio maps before and after the dipping for 30 min. It is considered that the acetone, IPA, ethanol dipping did not influence the Br-doping.

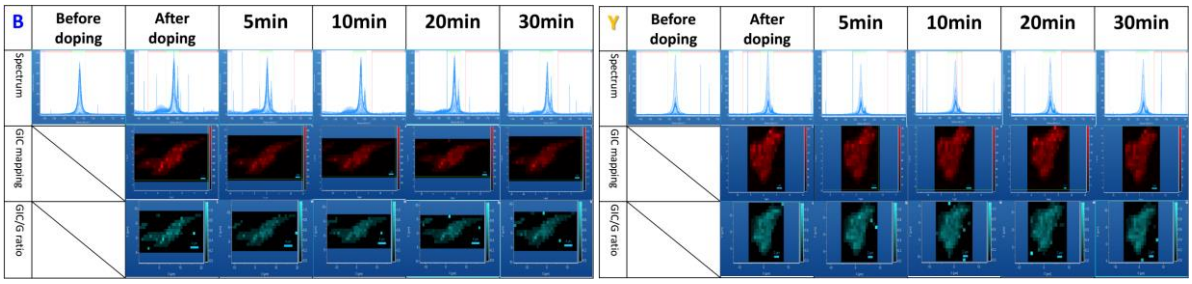
On the other hand, according to **[333]**, Br-intercalated MLG forms a "residue" compound in air and is chemically stable over time. The entire inductor fabrication process includes hard baking of SU-8 polymer dielectric in 200 °C in air for 20 minutes. No

degradation was observed for the Br_2 doping, indicating that GIC is also thermally stable.

Acetone (several 10 nm) **Acetone (several 100 nm)**



IPA (several 10 nm) **IPA (several 100 nm)**



Ethanol (several 10 nm) **Ethanol (several 100 nm)**

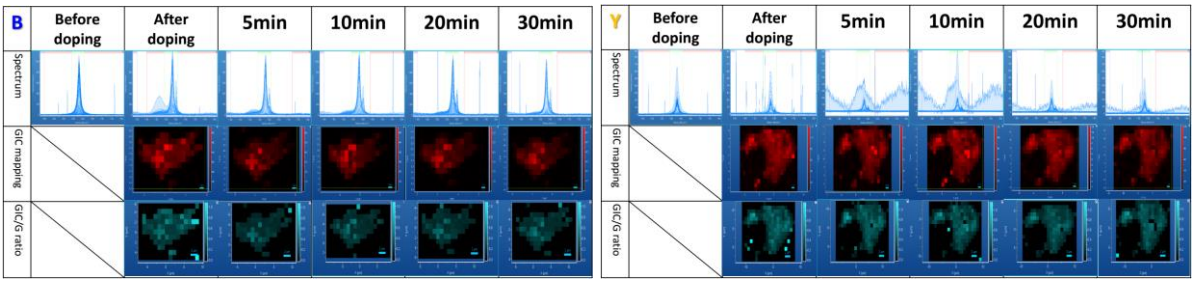


Figure 183: Study of Stability.

Raman spectra, GIC peak mapping and GIC/G ratio mapping of doped MLG samples before and after dipping for 5, 10, 20 and 30 min. All spectra are measured with 532 nm laser.

5. Scattering Parameter Simulation

The quality factor (*Q*-factor) of an inductor is the ratio of its inductive reactance to its resistance at a given frequency, and is a measure of its efficiency **[58]**. It is an important metric in high-performance RF/mixed-signal circuits, which has to be optimized simultaneously w.r.t. its size (or design) and fabrication cost. To accomplish a superior design, it is very important to correctly understand the effect of each inductor parameter on the inductor performance. Also, simulations are essential to analyze and interpret the experimental results.

It is worth noting that simulation of MLG inductors is difficult under the current state of advance in modeling/simulation of inductance of carbon nanostructures. There is no commercial electromagnetic (EM) simulator that has the designed capability to capture the intrinsic physical mechanism and then model the impedance/inductance of carbon nanomaterials. Due to the unique atomic structure and dispersion relation of graphene, the impedance behaves quite differently from that of conventional metals. In fact, we have tried simulations of graphene-based inductors using EM tools such as ANSYS HFSS **[405]** by using "equivalent electrical conductivity". However, all the tools failed because they cannot go beyond the simplifying assumptions of Ohm's law and failed to consider the effects of electric-field variation within a mean free path and current dependency on the nonlocal electric-field for graphene **[267]**. Hence, such simulation is beyond the scope of this manuscript.

However, simulation based optimizations of varieties of inductors based on conventional metals (copper and silver) are possible and can be performed for reference prior to design and fabrication. These simulations were implemented using ANSYS HFSS, which is a commercial software relying on the finite-element method (FEM) for solving Maxwell

equations. Considering this full-wave electromagnetic simulation technique, on-chip inductors are modeled as equivalent bulk coils with electrical conductivities incorporating grain-boundary and surface-scattering effects in micro- and nano-scale for metals **[406]**, and conductivities extracted from DC measurements for graphene. The conductivities with consideration of size effects for Cu and Ag are 48.46×10^6 and 50.97×10^6 S/m, respectively. Subsequently, the full inductor models were built in the software according to the actual physical structures that we fabricated, as shown in **the figure below**.

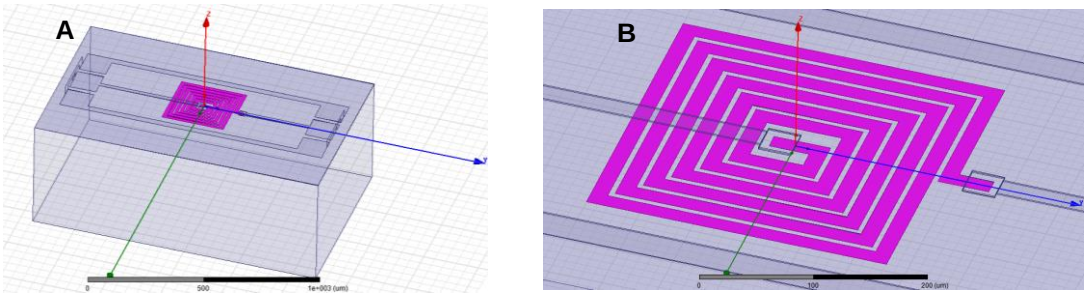


Figure 184: ANSYS HFSS simulation.

An inductor model (A) built in ANSYS HFSS for simulation, and (B) zoomed view of the inductor coil in (A).

Due to the high maturity of such commercial simulator for simulating conventional inductors, the simulations of metal-based inductors gives very close results to experimental measurements of metal-based inductors, as shown in **Figure 185** and **Figure 186**. The metal inductor was fabricated by the same process flow as MLG inductors other than that the metal spiral part was realized using a lift-off process. The main reason for the small difference is that there is a thickness variation with the deposited thickness of conductor and

the fabricated device is slightly thicker than the design. Hence, it is reasonable to use simulation data of metal-based inductors for comparison with intercalated MLG inductors later in this study.

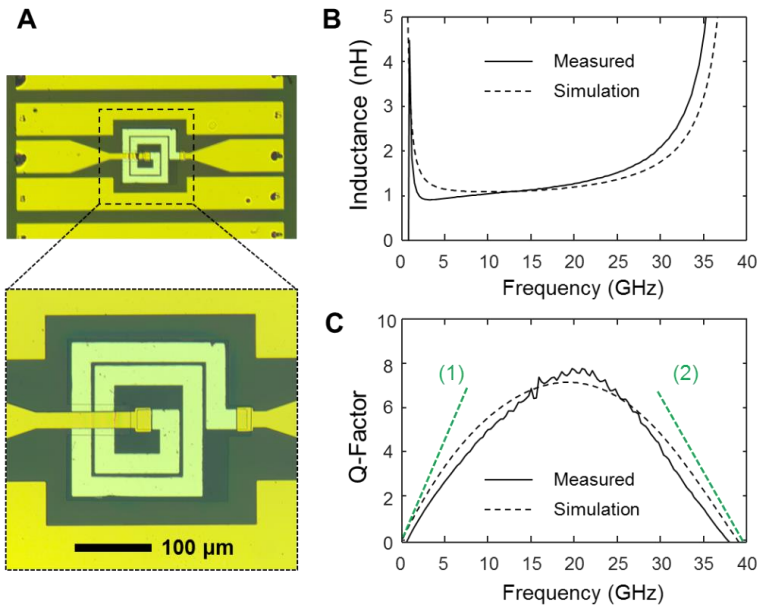


Figure 185: Comparison of simulation and experiment of Cu inductors.

(A) Microscope image of a 2-turn metal (Ag) inductor with 200 μm diameter, 200 nm spiral thickness and 1 μm thickness of SU-8 dielectric. (B) Inductance vs. frequency plot and (C) *Q*-factor vs. frequency plot of the 2-turn inductor in (A). (solid black curve: measured; broken black curve: simulated). Green dash lines represent (1) the $\omega L/R_S$ upper limit of *Q*-factor, and (2) substrate loss, self-resonance and skin effects at high frequencies.

Then the scattering parameter data as well as the *L* and *Q* for Cu based inductors are calculated using the same approach, which will be used later for the benchmarking of intercalated MLG inductors with Cu inductors. The structures are assumed to be the same as that of intercalated MLG inductors (2-turn layouts with an outer diameter of 200 μm, inter-

turn distances of 5 – 10 μm, SU-8 dielectric layer with thickness of 2 μm). A bunch of example data for the 2-turn octagonal layout are show in **Figure 187**, with varied thicknesses. It can be observed that by tuning the spiral thickness, a trade-off between *L* and *Q* can be realized. As the design rules of any inductor, no inductor layout is optimal for all the high-frequency range and more inductor turns typically lead to higher inductance values but to lower operation frequencies. The 2-turn designs turned out to work mainly in the 10 – 50 GHz frequency range.

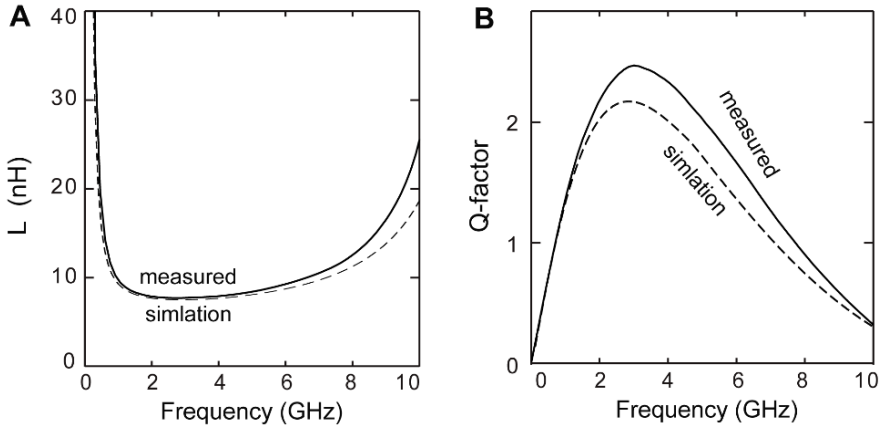


Figure 186: Comparison of simulation and experiment of Ag inductors.

(A) Inductance vs. frequency plot and (B) *Q*-factor vs. frequency plot of a 6-turn inductor based on metal (Ag) with 200 nm thickness (solid curve: measured; broken-curve: simulated).

6. Fabrication of Intercalated MLG Inductors

Two different fabrication process flows based on *doped-before-etching* method and *doped-after-etching* method were proposed, respectively. The *doped-before-etching* process was adopted due to its better results compared to that of *doped-after-etching* method.

For *doped-before-etching* method, as shown in **Figure 188**, HOPG slices were first transferred onto quartz substrates (1 cm × 1 cm × 1 mm), followed by Br intercalation doping. Doped flakes were patterned into spirals using oxygen inductive coupled plasma.

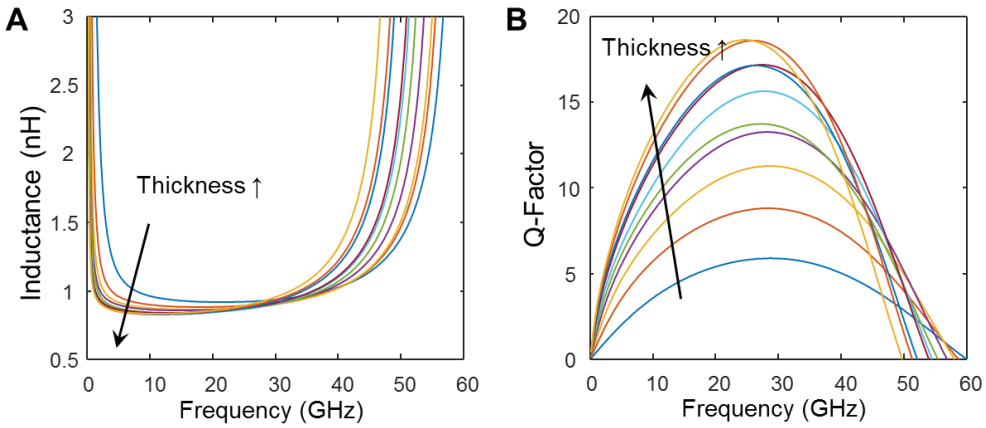


Figure 187: A bunch of example data for the 2-turn octagonal layout.

(A) Inductance vs. frequency plot and (B) *Q*-factor vs. frequency plot of the 2-turn octagonal inductor based on metal (Cu) with various thickness (100-1000 nm).

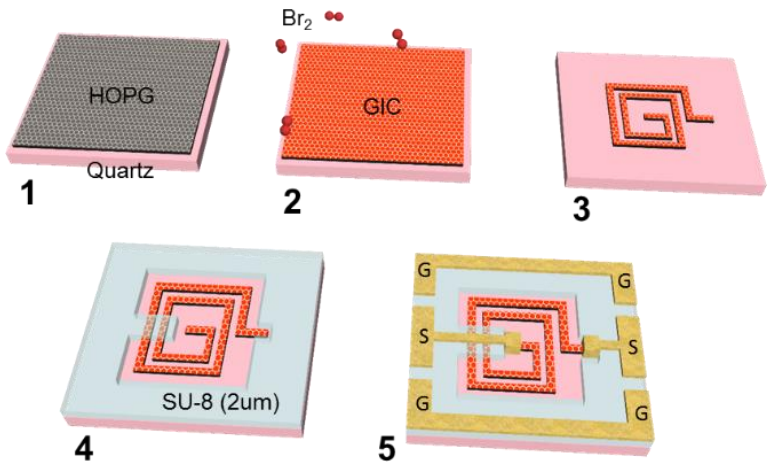


Figure 188: Fabrication process of intercalated MLG on-chip spiral inductors.

The intercalated MLG flakes were patterned into spiral inductor coils using photolithography followed by oxygen inductive coupled plasma. In this work, a set of 2-turn layouts with an outer diameter of 200 μm were designed as examples for demonstrating the intercalated MLG technique (**Figure 189e-g**). Such layout is typical for conventional metal inductors as well, and it works mainly in the 10 – 50 GHz frequency range, which covers various aspects of IoT, such as Wi-Fi, wireless USB, 4G/5G mobile networks, radar and satellite communications. For comparative study, three slightly different layouts have been designed – *octagonal* shape (**Figure 189e**), *narrow square* shape (**Figure 189f**) and *wide square* shape (**Figure 189g**). The inter-turn distances are 5 μm, 10 μm, 5 μm for the three layouts, respectively, which provide the optimal L_M, and C_S, and hence optimal *Q*-factors for each layout.

Then SU-8 photoresist was spin-coated, patterned and hard baked (180℃) to form a permanent low-*k* polymer dielectric layer with thickness of 2 μm and a relative permittivity of 3.1, serving as the isolation layer between inductor coils and the overlap metal pads.

Subsequently, metal contacts and pads (Ni/Au: 10 nm / 2000 nm) were deposited and patterned. The metal pads are designed as ground-signal-ground (GSG) coplanar waveguide (CPW) **[398]** structures with intercalated MLG inductor in the signal path for 2-port scattering parameter (S-parameter) measurements (**Figure 189e-g**). It is worth noting that in order to ensure the transport of the transverse electromagnetic mode in the CPW, the two GSG ports (indicated by “G” and “S”) have to be far away from each other. It can also suppress the higher-order modes, which can radiate and affect the results.

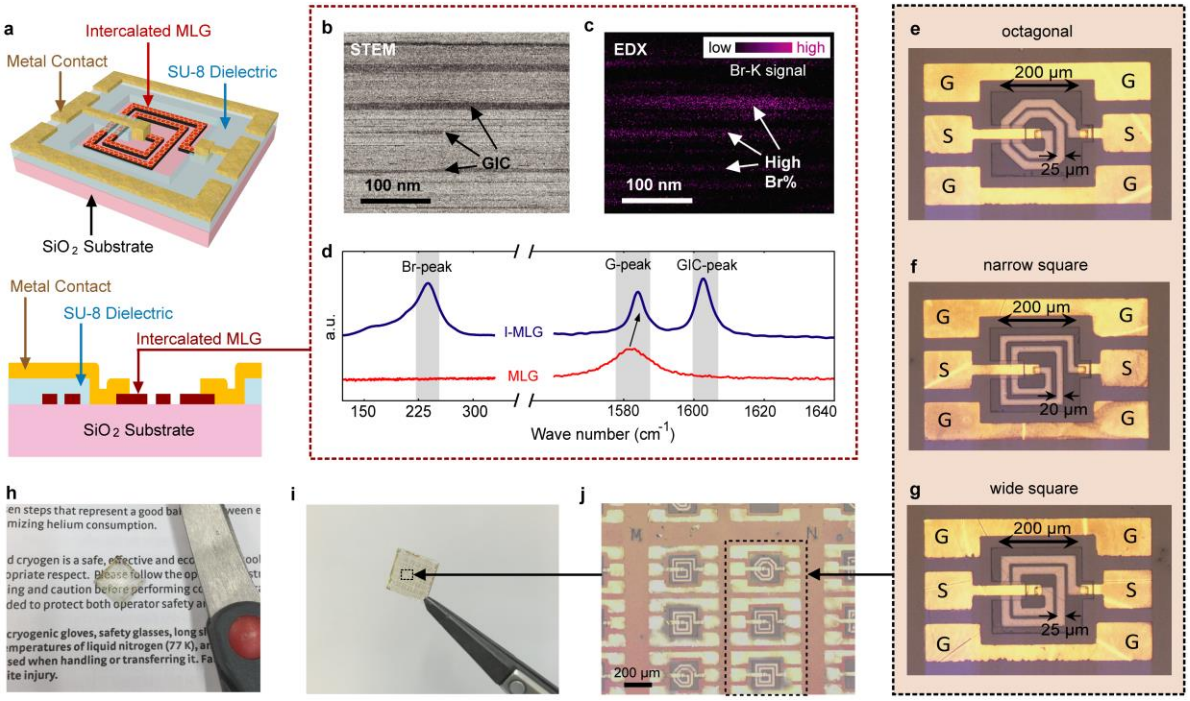


Figure 189: Design of Br intercalated graphene inductors.

Schematic of the 2-turn inductor design: top: perspective view; bottom: cross-section view. (b) STEM images of the cross section of the intercalated MLG showing the randomly distributed doping. (c) EDX images of bromine-K signal from the same region in (b). (d) Raman spectrum before and after Br-intercalation. (e-f) Optical images of (e) octagonal, (f) narrow square and (g) wide square intercalated MLG on-chip inductors. G and S represent the ground line and signal line of the GSG CPWs, respectively. (h, i) Photos of a fabricated chip with intercalated MLG inductor arrays (h) clamped by tweezers and (i) placed on paper. (j) Optical microscope image of an inductor array.

To demonstrate the repeatability and to find the thickness dependence, 28 intercalated MLG inductors with different thicknesses (different series resistances) were fabricated on the same 1 cm × 1 cm die. **Figure 189h** and **Figure 189i** show the entire chip and **Figure**

189j shows a micrograph of an intercalated MLG inductor array on the chip.

7. S-Parameter Measurements

Subsequently, S-parameter measurements were performed in the frequency range of 100 MHz – 67 GHz using Agilent N 5227A Network Analyzer and a microwave probe station equipped with Cascade Infinity GSG-probes with 150 μm pitch size (**Figure 190**). To capture the intrinsic properties of the MLG inductors themselves, a standard de-embedding procedure was performed to remove the parasitic effects of the CPW metal pads using dummy (open) structures (GSG CPWs without MLGs on the signal path) fabricated on the same chip, which is sufficient for devices operated below 50 GHz.

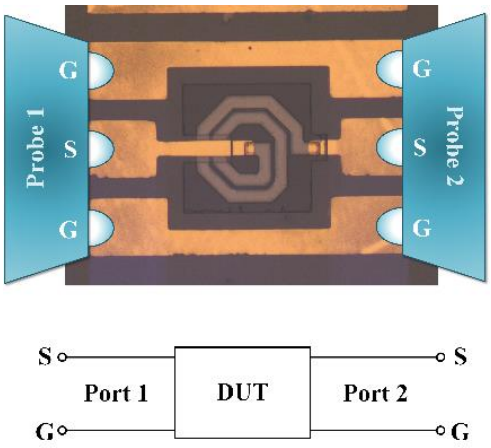


Figure 190: Schematic showing S-parameter measurement.

As shown in **Figure 191**, because the input impedance of the graphene device is smaller than that of the dummy (open) structure, there are smaller signal reflection (S_{11}) and larger transmission (S_{12}) in the graphene device.

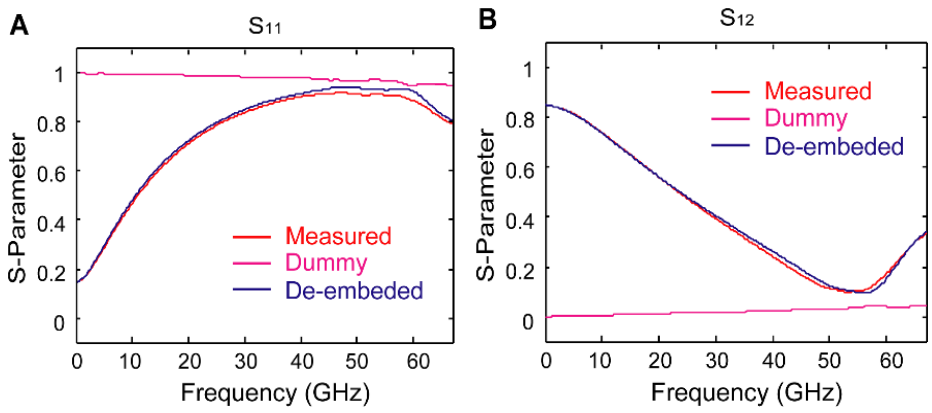


Figure 191: Magnitude of S-parameters.

(A) reflection characteristics S_{11} and (B) transmission characteristics S_{12} of a 2-turn doped MLG inductor based on intercalated MLG.

The admittance parameters (Y-parameters) for MLG inductor samples can then be calculated using these equations **[407]**:

$$\begin{cases} Y_{11} = \left((1-S_{11})(1+S_{22})+S_{12}S_{21}\right)/\Delta s \\ Y_{12} = -2S_{12}/\Delta s \\ Y_{21} = -2S_{21}/\Delta s \\ Y_{22} = \left((1+S_{11})(1-S_{22})+S_{12}S_{21}\right)/\Delta s \end{cases} \quad (42)$$

where $\Delta s = (1+S_{11})(1+S_{22})-S_{12}S_{21}$.

Then the inductance L and the Q-factor can be calculated as $L = -(2\pi f \,\mathrm{imag}(Y_{11}))^{-1}$ and $Q = -\,\mathrm{imag}(Y_{11})/\mathrm{real}(Y_{11})$, respectively, where f is the frequency, Y_{11} is the input admittance of port 1 with port 2 shorted, converted from S-parameters, and real/imag denotes the real/imaginary part, respectively.

8. Inductance and *Q*-Factor

Comparisons of L and Q between the intrinsic MLG inductors and the intercalated MLG inductors were first performed and shown in **Figure 192**. In each subfigure, a pair of

undoped and doped devices with similar thickness are compared. It can be seen that the L of the undoped devices are less than 1 nH around the operation frequency range (30-50 GHz). With Br intercalation doping, a significant improvement of both L and Q can be seen in all the three layouts. The improvement of L is mainly due to the band structure engineering – a interlayer decoupling effect from layer separation by intercalation doping, where the energy dispersion of MLG changes from hyperbolic form to the linear form as in few-layer or monolayer graphene. According to **Figure 125**, this band structure engineering can improve L_K of MLG. The improvement of Q is a combined effect of both the band structure engineering (improving L_{total}) and the doping effect (increasing carrier density leading to reduced series resistance R_S), since the upper bound of Q-factor is proportional to L_{total}/R_S.

In the previous section, we have shown graphene inductors with extremely small diameters (tens of um) and small thicknesses (tens of nm), thereby applicable for extremely high operation frequency (around 50 GHz) and low Q that are unsuitable for practical RF applications. High inductance density up to 1650 nH/mm² was found from them even without doping, which is due to the extreme dimensions. According to the analysis above, that inductance density can be further improved if doping is applied.

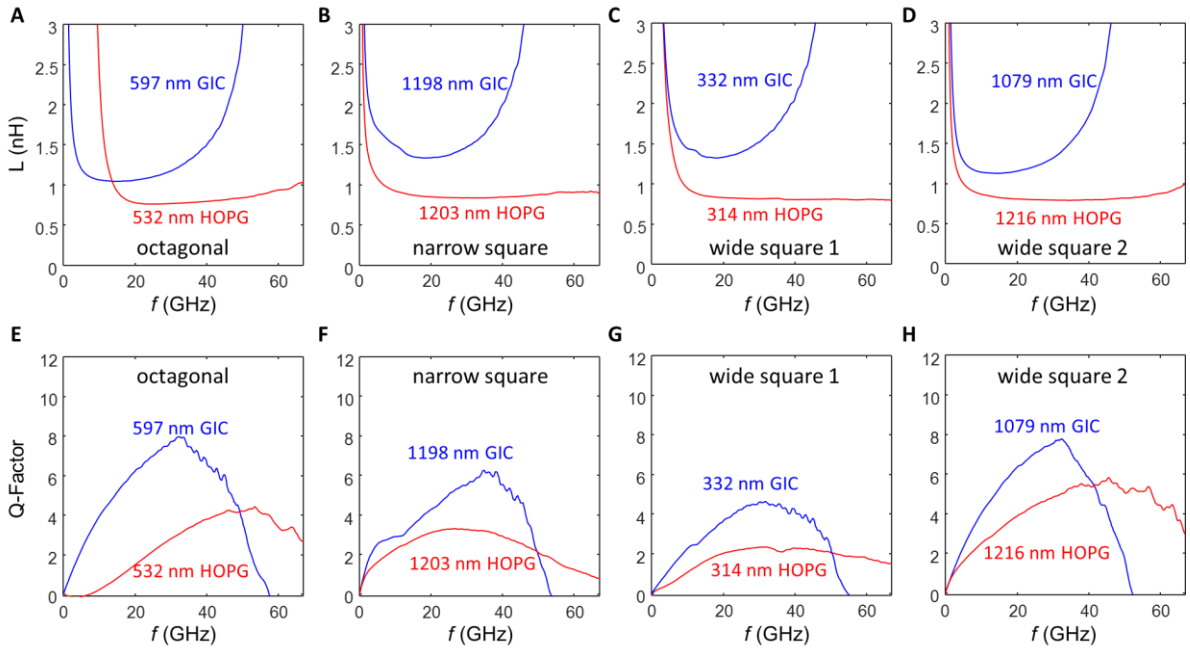


Figure 192: Q-factor and inductance vs. frequency with and without intercalation. (A-D) Q-factor vs. frequency plots of (A) *octagonal*, (B) *narrow square* and (C,D) *wide square* 2-turn inductors based on undoped samples (HOPG) and doped samples (GIC) with similar thicknesses. (E-H) inductance vs. frequency plots of (E) *octagonal*, (F) *narrow square* and (G,H) *wide square* 2-turn inductors based on undoped samples (HOPG) and doped samples (GIC) with similar thicknesses.

Measured *Q*-factor vs. frequency for one sample in each layout is plotted in **Figure 193**, compared with Cu inductors with the same series resistance, layout, and substrate. It can be seen that all the three designs can provide a maximum *Q*-factor around 10, which is sufficient for many on-chip inductor applications **[408]**. The maximum *Q*-factor is about 12 for one of the *narrow square* inductors with a series resistance of 10 Ω (**Figure 193b**). It is obvious that with the same series resistance, both higher *L* and higher *Q* compared to that of Cu are achieved by intercalated MLG. Due to the negligible skin effect under 60 GHz in these inductors (the current distribution in the cross-section is uniform in both Cu and

MLG), the L_M is almost identical in Cu and MLG, which is primarily due to the same layout design. Hence, the source of the extra inductance value in intercalated MLG compared to Cu can only be attributed to the kinetic inductance L_K.

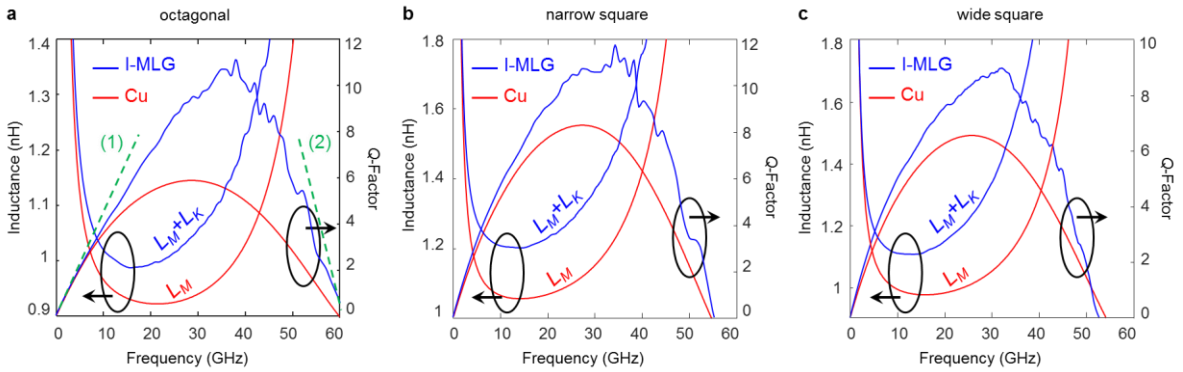


Figure 193: Measured inductance and *Q*-factor vs. frequency.

Three intercalated MLG (I-MLG) inductors in different layouts are compared to Cu inductors: (a) octagonal, (b) narrow square and (c) wide square layouts. In each sub-figure, the I-MLG and the Cu inductors compared have the same series resistance, same layout and substrate. The series resistances are 14 Ω, 10 Ω and 28 Ω for (a), (b) and (c), respectively, since (a), (b) and (c) have different layouts and spiral thicknesses. Green dash lines in (a) represent (1) $\omega L/R_S$ upper limit of *Q*-factor and (2) substrate loss, self-resonance and skin effects at high frequencies. See Supplementary Information 4 for more details about these two lines.

The measured inductance (density) vs. maximum *Q*-factor plots for all the 28 intercalated MLG inductors are shown in **Figure 194**. Generally thinner inductors have higher inductance (due to slightly lower inter-turn capacitance, and much higher L_K) and lower *Q*-factor (due to higher series resistance), while thicker inductors have higher *Q*-factor and lower inductance. Hence, by tuning the spiral thickness, a trade-off between *L* and *Q*

can be realized (inset in **Figure 194a**). Overall, there is no significant difference among the three layout designs in terms of *Q*-factors, excepting that the narrow square inductors have slightly more scattered *Q*-factors because of larger doping degradation variation for narrower width (**Figure 194b**).

Compared to Cu inductors, it is clear that the same *Q*-factors can be easily achieved using intercalated MLG. More importantly, for all the three layout designs, the inductance values are always much better than Cu when the same *Q*-factors are achieved. As shown in **Figure 194**, without compromising *Q*-factors, up to 1.5x higher inductance density can be achieved by intercalated MLG inductors. As discussed above, the extra inductance value in MLG compared to Cu is contributed by its high kinetic inductance L_K, which is up to 50% of the L_M. In other words, in RF circuit designs, the area required to provide the necessary inductance value can be reduced by up to one-third (estimated as required area = required inductance / inductance density).

Vice versa, when the same inductance density is achieved by both intercalated MLG inductor and Cu inductor, the intercalated MLG inductor exhibits much higher *Q*-factor. One can also choose specified *L*-*Q* points on the blue curves in **Figure 194** to achieve a combination of both higher *L* and higher *Q* compared to that of Cu, as illustrated by the dotted arrowed lines in **Figure 194b**. Hence, compared to Cu based inductors, there is a clear advantage of the intercalated MLG inductors in terms of inductance density as well as *Q*-factors: the high *L* – high *Q* combination that could never be achieved simultaneously in a given layout with conventional metals such as Cu, have been achieved with intercalated MLG. It is obvious that intercalated MLG on-chip inductors are closer to the top right "desired direction" illustrated in **Figure 194**.

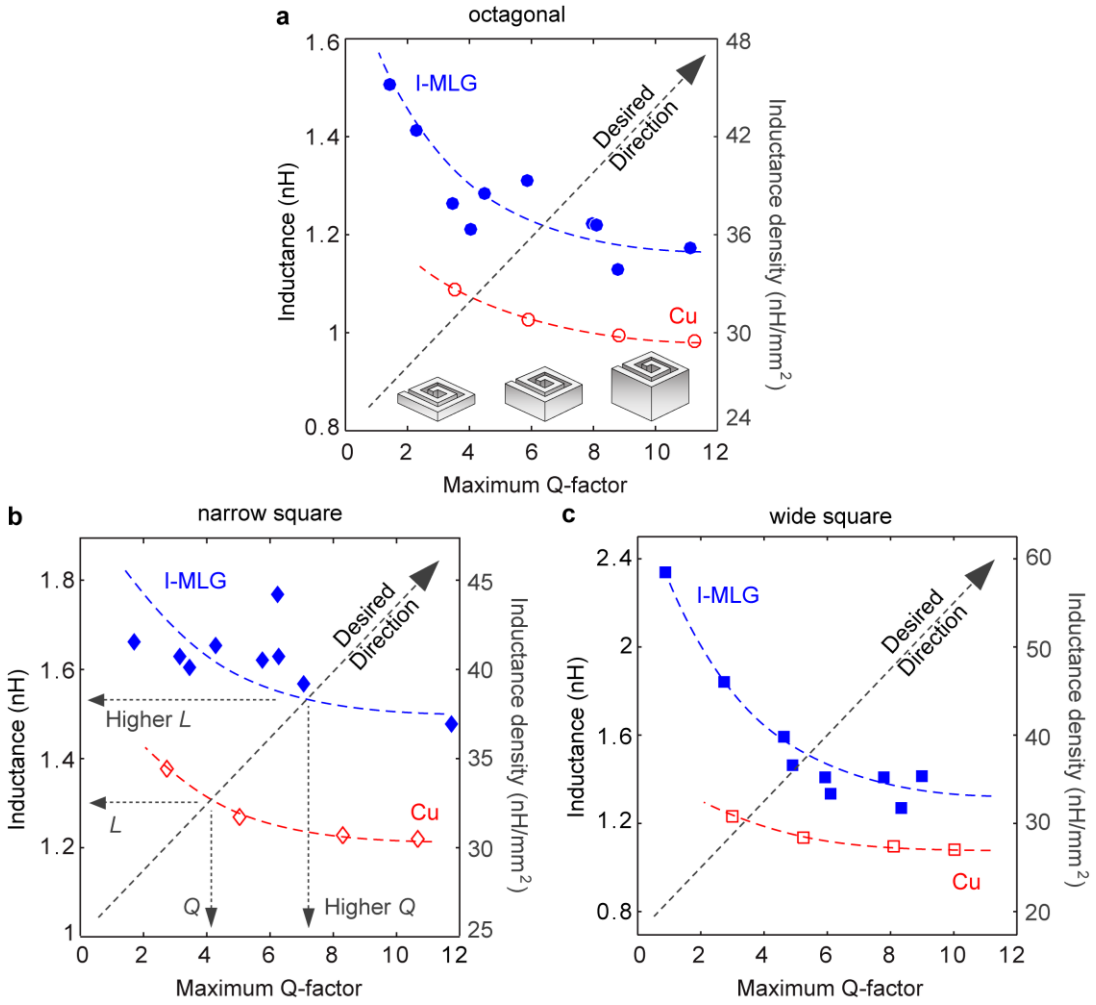


Figure 194: Comparison of intercalated MLG and Cu inductors.

Plots of inductance (and the corresponding inductance density) *vs*. maximum *Q*-factors of intercalated MLG and Cu inductors for (a) *octagonal*, (b) *narrow square* and (c) *wide square* 2-turn layouts. Symbols represent data points, and dashed curves are drawn for visual guidance only. Inset in (a) indicates that the *L*-*Q* trade-off is realized by tuning spiral thickness. For each device, the inductance (density) is extracted at the frequency where the maximum *Q*-factor is found (typically around 30 GHz). Cu data are calculated by HFSS and calibrated with experiments (see Supplementary Information 7).

As mentioned in the previous section, the average intercalation stage in the samples is 3. However, further improvement in both L and Q is expected if stage-1 intercalation can be achieved. There are also other intercalation guests that can induce higher and/or more stable doping compared with Br **[15], [333]**. Moreover, the Q-factors can be further increased by improvement of the contact quality **[17]**. Hence, with advancements in graphene intercalation technology and contacts, improvements in both Q-factors and L can be expected.

In conventional metal inductors, reducing the size/area of the spiral reduces the amount of magnetic flux that is proportional to the "surface area" of the individual spiral segments as well as the area enclosed by each turn of the spiral. This reduces the magnetic inductance and can also induce severe "size effects" (such as quantum confinement that worsens the electronic structure, as well as surface, edge and grain boundary scatterings) **[16]**, when the dimensions are scaled down to tens of nanometers. Due to such effects, electrons are less mobile in nano-scale metals, leading to a sharp non-linear decline in the metal conductivity and thereby in the Q-factor. Hence, dimension scaling of metal inductors is not sustainable. Remarkably, MLG has no severe size effects when the thickness and width are scaled down to tens of nanometers **[15]**. This is because the unique electronic structure allows electrons/holes to move with minimal resistance in quantum-confined layers, and because of its 2D nature where the pristine interfaces minimize the roughness and scattering of the surfaces **[57]**. On the other hand, the kinetic inductance becomes more and more dominating (since L_K scales as L_K/N) with thickness and width reduction of MLG. Hence, in case of any further scaling, MLG can harvest more inductance density without degrading the conductivity, compared to conventional metals. Such scalability of MLG can be further enhanced by intercalation, and can be highly beneficial for designing "ultra-compact" and

"ultra-thin" passives including on-chip inductors and antennas for future wireless communication systems.

D. Chapter Summary

1. Chip Area Reduction

We demonstrated a fundamentally different on-chip inductor to significantly improve inductance density and thus area-efficiency, without compromising performance, by exploiting the unique characteristics of intercalated MLG. By using Br intercalation as an example, the demonstrated intercalated MLG based on-chip inductors exhibit undiminished *Q*-factors up to 12 and up to 1.5x higher inductance density than that of Cu inductors with the same footprint, which translate to an inductor area reduction by about one-third.

An example of chip-area reduction is provided using an example of a phase-locked loop (PLL) that are widely employed in high-speed and high-frequency data communication systems required in almost all wireless electronic applications. One of the important building blocks of the PLL is the Voltage-Controlled Oscillator (VCO). To demonstrate the possible application of the graphene inductors in such systems, a VCO using graphene inductors needs to be designed and simulated. The primary goal in the design of a VCO is to design active devices to overcome the losses associated with the LC parallel resistance. A cross-coupled differential VCO shown is designed in **Figure 195A**. It consists of three components: LC tank, tail bias current source, and a cross-coupled differential NMOS pair. The LC tank is made by a pair of graphene inductors and a pair of capacitors connected in parallel. The capacitors are sized to ensure a desired resonance frequency ($1/2\pi\sqrt{LC}$). The cross-coupled transistors provide the negative input resistance. The input resistance of the cross-coupled transistors (R_{in}) is given by $R_{in}= -2/g_m$, where g_m is the small signal

transconductance of each NMOS. This negative resistance is used to offset the positive resistance in the passive components (LC tank), to produce an oscillation, and hence the transistors are sized accordingly and realized in CMOS process.

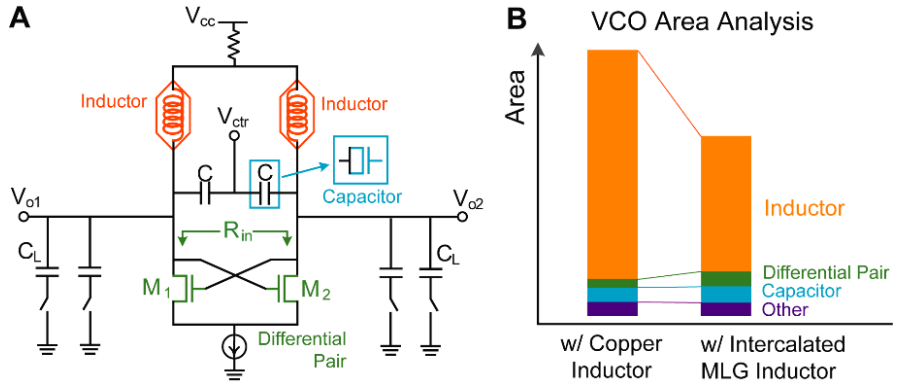


Figure 195: Area Reduction Achieved by MLG Inductors.

(A) Circuit diagram of a CMOS cross-coupled LC voltage-controlled oscillator (VCO) using graphene inductors. Each capacitor is realized by a MOSFET (source and drain are connected as one terminal). (B) Area analysis of the circuit in (a), compared with the same circuit with Cu inductors.

Assume a larger differential pair is used in order to provide a larger negative resistance to cancel out any possible increase in series resistance (i.e. metal-graphene contact resistance). Although the chip area occupied by the differential pair is increased, however, its area is still not comparable to that of the inductors. The area reduction for the inductors due to the high inductance density of intercalated MLG is much more significant, resulting in a reduction in the total area of the VCO circuit, as illustrated in **Figure 195B**.

Most importantly, a die area decrease translates into more dies fabricated on a wafer, which in turn implies a lower die cost. Assume an RF chip with 40% area taken by

inductors. If the inductor area can be reduced by a factor of 2 (50% reduction of inductor area translates to 20% reduction of chip area), according to **[362]**, we can estimate that a chip area reduction of 20% results in a cost reduction of 23%, for a die area of 1 cm^2.

2. Compatibility with State-of-the-Art Technologies

Because of the fact that the technique is a purely materials based approach, which does not solely rely on the magnetic field, our approach is compatible with various structural design techniques such as multilayer/3D inductor structures, rolling-up and/or use of magnetic cores/dielectrics. Hence, it can be used in many state-of-the-art inductors to further improve performance and form-factors. In addition, the approach is useful for the alleviation of unwanted electromagnetic coupling between neighboring inductors in scaled RF IC technologies, because kinetic inductance does not have any coupling or mutual component. The planar nature of 2D materials and the low temperature process enables the BEOL integration with current RF technologies with relative ease.

MLG inductors can be fabricated under low temperature processes (including room temperature transfer, doping and patterning) which are within the BEOL thermal budget (400-600℃) of CMOS. Moreover, due to the feasibility of dry etching of MLG, there is no need for damascene process to define the pattern. Dielectric encapsulation of intercalated MLG in the BEOL environment can also increase the stability of intercalation doping. Additionally, the superior thermal conductivity of MLG w.r.t conventional metal materials can be exploited to alleviate on-chip hot-spots, and further improve performance and reliability of RF-ICs **[16]**.

One existing challenge for process integration is how to get rid of the wet transfer process, which is not desirable in state-of-the-art CMOS technologies. Efforts toward low-temperature graphene film growth on dielectric surfaces are needed. Another challenge is

how to form high-quality interfaces between MLG inductors and vias. One possible solution is the adoption of carbon-based vias (as illustrated in **Figure 196**), which can form homogeneous junctions with MLG. Work toward such goal include aligned carbon nanotubes perpendicularly contacting with MLG **[409]**, and the graphenic carbon contacts **[410]**.

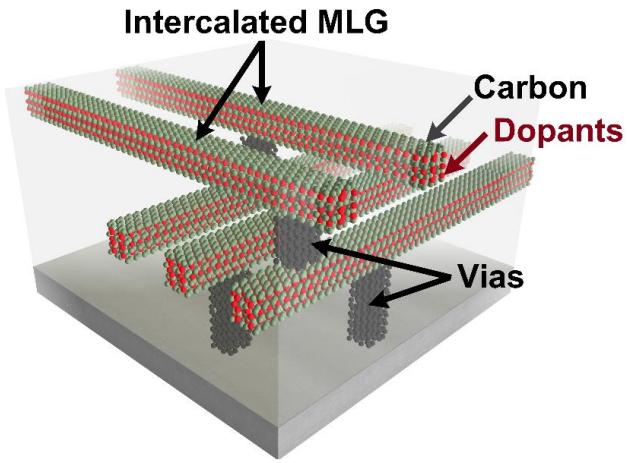


Figure 196: Illustration of intercalated MLG integrated with carbon-based vias

3. Conclusion

Our demonstration paves the way for design and fabrication of graphene-based on-chip inductors for RF-IC applications, providing guidelines for future RF-IC design based on 2D materials, with significant implications for numerous applications in communication, sensing and energy storage/transfer. Combining the superb mechanical and optical properties of 2D materials, our demonstration can also open up new avenues in fabricating flexible/stretchable/wearable wireless electronics (for example, **Figure 197**) that are needed to realize the emerging paradigms of the *Internet of Things* and *Industry 4.0* (*Cyber-Physical Systems* – the 4th industrial evolution).

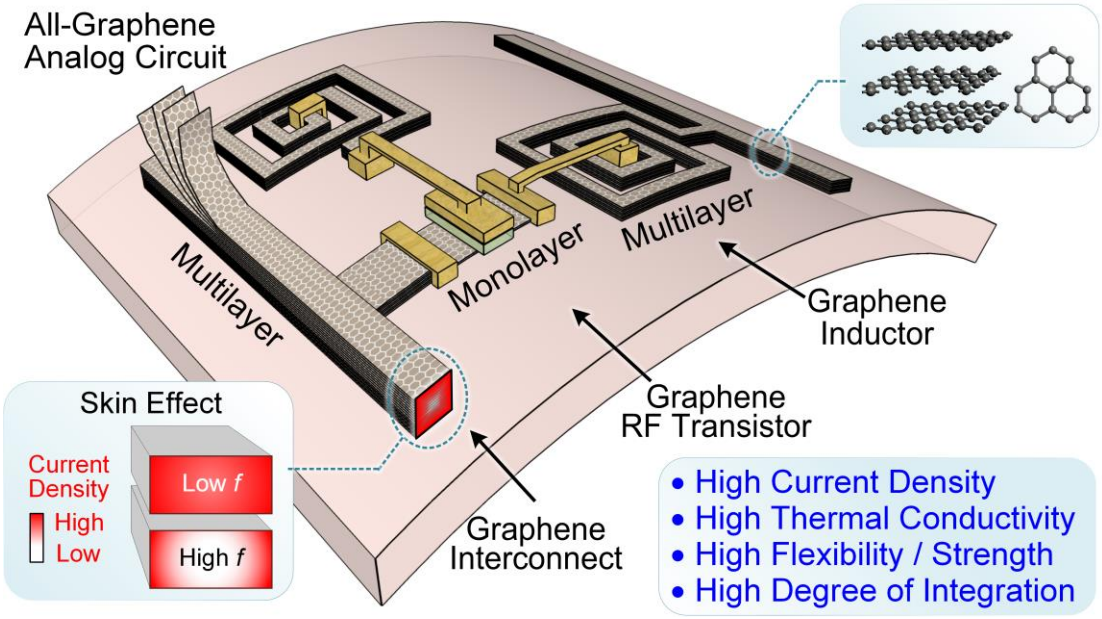


Figure 197: Schematic illustrating an all-graphene analog circuit

The figure shows a frequency mixer. All circuit components, including monolayer-graphene-based RF transistor, multilayer-graphene-based inductors and interconnects are monolithically integrated on a single flexible substrate. The extraordinary physical properties of graphene, as listed on the lower right hand side, make it an ideal material for future flexible electronics. The design and fabrication of graphene on-chip inductors constitute a key step toward the realization of such flexible circuits and systems.

VII. Quantum Transport in 2D Transistors

Performance evaluation of 2D-based FETs is a necessity in order to explore the feasibility and scalability of 2D semiconductors for future technologies. By employing quantum transport methods, the performances of 2D MOSFETs **[31], [411]** and 2D TFETs **[48]** for sub-10 nm technology nodes have been benchmarked. However, the projection of memory access transistors is still lacking. The major challenge is that an important leakage mechanism – gate-induced drain leakage (GIDL) needs to be carefully modeled in quantum transport regime, by capturing all the essential physics of scattering and tunneling, which has not been done previously.

GIDL is one of the main leakage mechanisms in field-effect transistors (FETs), especially access transistors that are widely employed in a variety of memory technologies. In this chapter, GIDL in emerging two-dimensional (2D) FETs is evaluated for the first time, by employing a novel dissipative quantum transport methodology based on Büttiker probes with band-to-band tunneling capability. It is shown that 2D semiconductors with relatively large bandgaps and favorable effective masses compared to that of silicon can greatly reduce GIDL, which is a compelling reason for using such materials in future memory technologies. Materials and device design considerations are discussed for minimizing the GIDL current. This work also provides guidelines for performance/scalability analysis of low-leakage applications of 2D FETs.

A. Introduction

GIDL is one of the key leakage mechanisms in MOSFETs **[412]** (**Figure 198a**) describing that at high drain biases in an overdriven off-state, the steep band bending near drain-channel junction allows conductive band-to-band tunneling (BTBT) that creates

excess leakage current. Historically, GIDL only referred to the vertical BTBT in gate-drain overlap region, but not the horizontal BTBT included in the reverse-bias leakage of the drain-body junction (**Figure 198b**). However, usually both BTBTs are clubbed together as GIDL **[413]**, because they are hard to differentiate when the body thickness is scaled. Moreover, GIDL can also be amplified by a parasitic bipolar transistor (PBT) effect (**Figure 198c**) **[414]**, where the drain, source and body work as collector, emitter, and base, respectively. Holes generated by BTBT at drain flow into the body by lateral electric field, thus increasing the body potential and turning on the source-body (emitter-base) p-n junction. Subsequently electrons are injected from source (emitter) to the drain (collector) as excess leakage current. The GIDL-PBT effect is more severe in conventional MOSFETs, wherein thicker semiconductor body allows more room for parasitics.

GIDL is undesirable for most FETs, especially memory access transistors, a group of transistors used in many charge-based memory applications including both volatile and non-volatile types **[415]** (**Figure 199a**). This is because these devices, when turned off, need to keep the charge stored in the cell as long as possible, and hence low off-current (I_{OFF}) leakage is more important compared to low subthreshold swing (SS) and high drive current, and therefore they are not scaled as much as logic devices. Hence, relatively large length, drive voltage and gate voltage swing are usually used for access transistors (**Figure 199b**), which induce significant BTBT and thus GIDL.

FETs based on two-dimensional (2D) semiconductors such as MoS_2 **[23]** and other transition metal dichalcogenides (TMD) (**Figure 199c**) can possibly minimize GIDL due to their relatively large bandgaps (E_g) and intermediate effective masses (m^*) compared to silicon, which suppress the BTBT probability **[45]** (**Figure 199d**), as well as their atomic scale thickness, which offers not only excellent electrostatics and scalability **[411]**, but also

minimizes PBT and eliminates vertical BTBT.

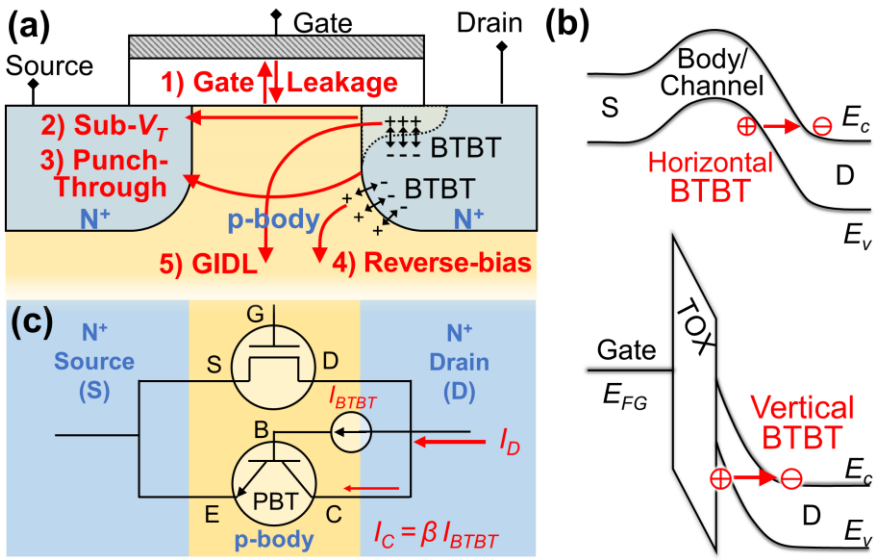
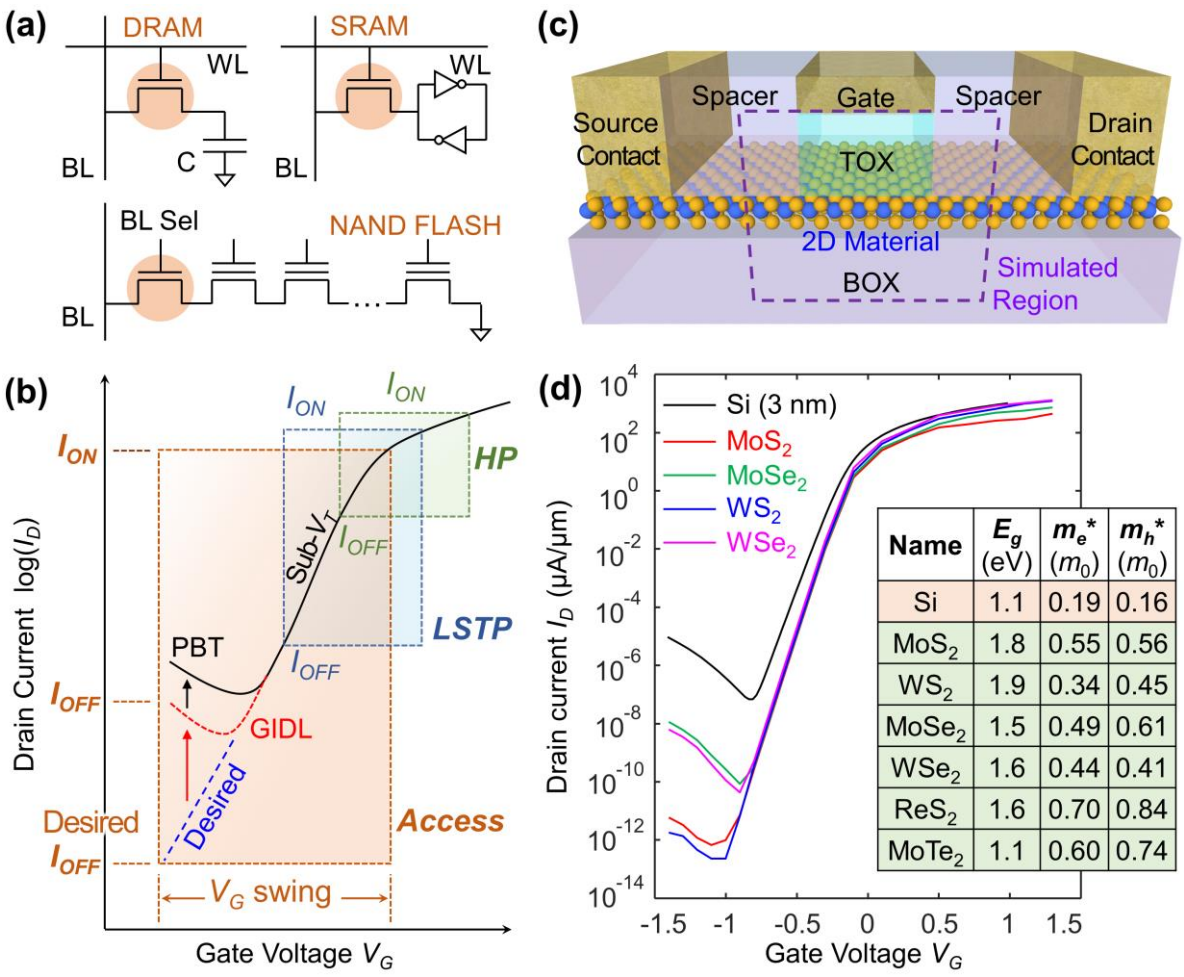


Figure 198: Main leakage mechanisms in a bulk MOSFET.

(a) Illustration of main leakage mechanisms in a bulk MOSFET, including: 1) gate leakages (F-N tunneling, direct tunneling and hot carrier injection); 2) subthreshold leakage (sub-V_T), and also source-drain direct tunneling; 3) punch-through leakage; 4) reverse-bias leakages, including impact ionization and horizontal band-to-band tunneling (BTBT); 5) gate-induced drain leakage (GIDL) due to vertical BTBT. Note that in advanced technologies with thin body, 4) and 5) are hard to differentiate and usually clubbed together as GIDL. (b) Band diagrams showing horizontal and vertical BTBT, where electrons (–) tunnel into E_c and leave holes (+) in E_v. (c) Illustration showing the parasitic bipolar transistor (PBT) effect where the BTBT leakage current (I_{BTBT}) is amplified by the PBT, thus increasing the total leakage current (I_D).



Name	E_g (eV)	m_e^* (m_0)	m_h^* (m_0)
Si	1.1	0.19	0.16
MoS_2	1.8	0.55	0.56
WS_2	1.9	0.34	0.45
$MoSe_2$	1.5	0.49	0.61
WSe_2	1.6	0.44	0.41
ReS_2	1.6	0.70	0.84
$MoTe_2$	1.1	0.60	0.74

Figure 199: Memory access transistors and opportunities for 2D materials.

(a) Circuit schematics of some charge-based random-access memory (RAM) technologies that utilize access transistors (in orange shades): dynamic RAM (DRAM); static RAM (SRAM) and NAND FLASH.

(b) Plots illustrating different I_D-V_G metrics for logic transistors in high-performance (HP) and low-stand-by-power (LSTP) technologies as well as access transistors in memory technologies. Access transistors commonly works with larger V_D and gate swing (i.e., larger V_{DG}), in which GIDL is more dominating for OFF current.

(c) Schematic of a FET based on 2D semiconductor, where TOX (BOX) is the gate (buried) oxide.

(d) I_D-V_G curves of fully-depleted silicon-on-insulator (SOI) FET with 3 nm silicon body and monolayer 2D TMD FETs, showing that GIDL can be much lower in 2D FETs. For both Si and 2D, a practical single top gate with gate (channel) length of 50 nm is assumed; TOX (BOX) is 5 (10) nm SiO_2; source/drain doping is 3×10^{26} m^{-3} (or 2×10^{17} m^{-2} equivalently for 2D materials); drain voltage V_D = 1.2 V. These parameters are within the typical ranges for a DRAM access device. These parameters are set as default values in the remainder of the paper if not mentioned. Inset table shows basic properties of some featured monolayer (1L) transition-metal dichalcogenide (TMD) semiconductors compared with silicon, which help reduce GIDL.

Therefore, performance evaluation of 2D-based FETs with consideration of GIDL is a necessity in order to explore the feasibility and scalability of 2D semiconductors for extremely low leakage applications. However, the reported modeling and simulations on 2D FETs in the past are mainly focused on logic devices with small biases according to ITRS **[411]**, and hence GIDL is not taken into account.

In addition, the commonly used "ballistic" transport is not applicable to 2D channels due to the inevitable scatterings. Hence, a novel device simulation scheme for 2D FETs that can capture both the dissipative transport scattering mechanisms and the BTBT effect is introduced in this work. Subsequently, GIDL in 2D FETs is evaluated for the first time. Design considerations for minimizing I_{OFF} including material properties and device geometry are discussed as well.

B. Quantum Transport for 2D

1. Quantum Transport

Recent works on modeling of nanoscale devices are mostly based on the sound conceptual basis of quantum transport, by a self-consistent simulation scheme, where Poisson's equation is solved to obtain the electrostatics, and transport equation is solved by non-equilibrium Green's function (NEGF) formalism **[275]** to get charge distribution. In such scheme, ballistic transport equation has been employed to study the upper-limit performance of MoS_2 FETs **[416]**. However, the inevitable phonon scattering keeps these devices away from being "ballistic" even at sub-10 nm nodes **[417]**. Moreover, besides phonon scattering, other scattering sources, such as electron-electron scattering, impurity/defect scattering, etc., may also be inevitable in practical device environment. Therefore, an approach based on the concept of "Büttiker probes" (**Figure 200a**) **[418] [419]** has been developed to treat the scattering events, which is capable of capturing all the essential physics of scattering, while being computationally efficient.

Similar to the effect of real scattering events, the "Büttiker probes" absorb carriers and desorb them back with disturbed momentum/ energy, but do not change the number of carriers passing by, i.e., net current at each probe remains zero.

2. A New Quantum Transport Scheme

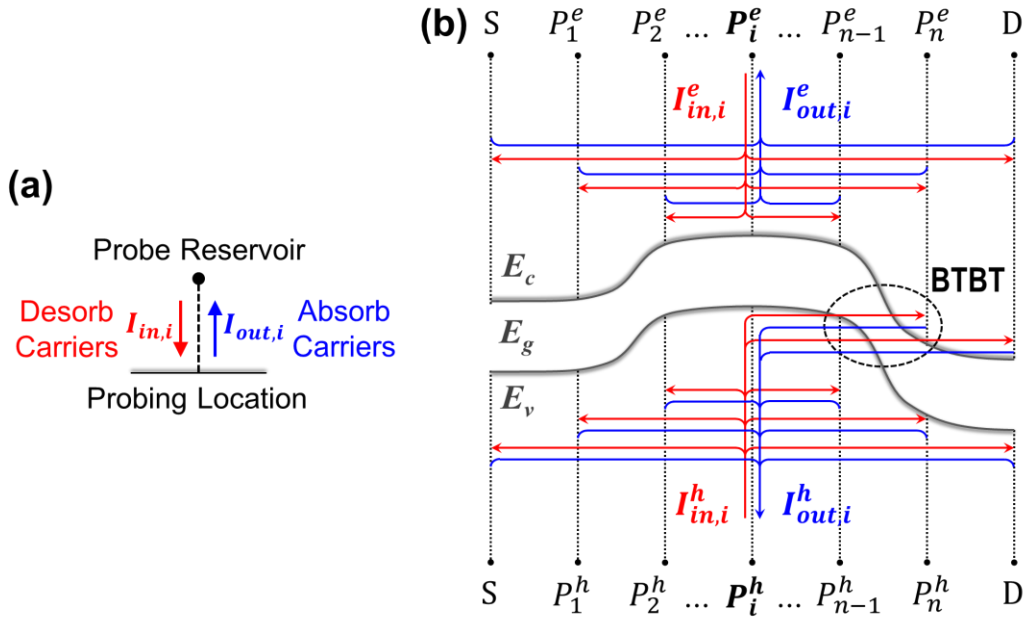


Figure 200: Proposed quantum transport methodology.

(a) The concept of Büttiker probes. Each probe P_i is a scattering center that can absorb carriers and then desorb them at a different energy from/to any other probes including the source (S) and drain (D). (b) Illustration of the proposed method using Büttiker probes in cooperation with two-band transport model plus BTBT, where two sets of probes are employed for electrons and holes, respectively.

However, the method above has only been used for one energy band **[411]**. Here we modified and applied it to both conduction band E_c and valence band E_v, as well as to the tunneling between them (**Figure 200b**) by employing two sets of Büttiker probes for electrons and holes, respectively. The modified current continuity equations with the variable intervals are:

$$I_{e,i} = I_{e,in,i} - I_{e,out,i} = \int_{-\infty}^{\infty} I_{e,i}\left(E_l\right) dE_l = 0 \tag{43}$$

$$I_{h,i} = I_{h,in,i} - I_{h,out,i} = \int_{-\infty}^{\infty} I_{h,i}\left(E_l\right) dE_l = 0 \tag{44}$$

where,

$$I_{e,i}\left(E_l\right) = \begin{cases} \dfrac{q}{\hbar^2}\sum_{\alpha}\sqrt{\dfrac{2m_{t,e}k_BT}{\pi^3}}\sum_j T_{\alpha}^{ij}\left[\mathcal{F}_{-\frac{1}{2}}\left(\mu_{Pe,i}-E_l\right)-\mathcal{F}_{-\frac{1}{2}}\left(\mu_{Pe,j}-E_l\right)\right] & 1)\textit{if } E_l \geq E_{mid,i} \\ & \textit{and } E_l \geq E_{mid,j} \\ \dfrac{q}{\hbar^2}\sum_{\alpha}\sqrt{\dfrac{2m_{t,eh}k_BT}{\pi^3}}\sum_j T_{\alpha}^{ij}\left[\mathcal{F}_{-\frac{1}{2}}\left(\mu_{Pe,i}-E_l\right)-\mathcal{F}_{-\frac{1}{2}}\left(\mu_{Ph,j}-E_l\right)\right] & 2)\textit{if } E_l \geq E_{mid,i} \\ & \textit{and } E_l < E_{mid,j} \\ 0 & 3)\textit{if } E_l < E_{mid,i} \end{cases} \tag{45}$$

$$I_{h,i}\left(E_l\right) = \begin{cases} \dfrac{q}{\hbar^2}\sum_{\alpha}\sqrt{\dfrac{2m_{t,h}k_BT}{\pi^3}}\sum_j T_{\alpha}^{ij}\left[\mathcal{F}_{-\frac{1}{2}}\left(E_l-\mu_{Pe,i}\right)-\mathcal{F}_{-\frac{1}{2}}\left(E_l-\mu_{Pe,j}\right)\right] & 1)\textit{if } E_l < E_{mid,i} \\ & \textit{and } E_l < E_{mid,j} \\ \dfrac{q}{\hbar^2}\sum_{\alpha}\sqrt{\dfrac{2m_{t,eh}k_BT}{\pi^3}}\sum_j T_{\alpha}^{ij}\left[\mathcal{F}_{-\frac{1}{2}}\left(E_l-\mu_{Pe,i}\right)-\mathcal{F}_{-\frac{1}{2}}\left(E_l-\mu_{Ph,j}\right)\right] & 2)\textit{if } E_l < E_{mid,i} \\ & \textit{and } E_l \geq E_{mid,j} \\ 0 & 3)\textit{if } E_l \geq E_{mid,i} \end{cases} \tag{46}$$

E_l is the longitudinal component (along channel length direction) of carrier energy; index i = 1, 2, …, n; index j = 1, 2, …, n, S, D; $\mu_{i/j}^{Pe(h)}$ is the Fermi level assigned to each probe, which is adjusted self-consistently to obtain zero net current at each probe; α is the transverse mode index; T_{α}^{ij} denotes the transmission between i and j with mode α; $E_{mid,i/j}$ is the mid-gap energy (in the middle of E_c and E_v); $F_{-1/2}$ is the Fermi-Dirac integral of order -1/2; m_t is the transverse effective mass (along channel width direction) defined in (c). $m_{t,e(h)}$ is the transverse effective masses of electrons (holes), while $m_{t,eh}$ is the BTBT-relevant reduced effective mass of electron-hole pairs.

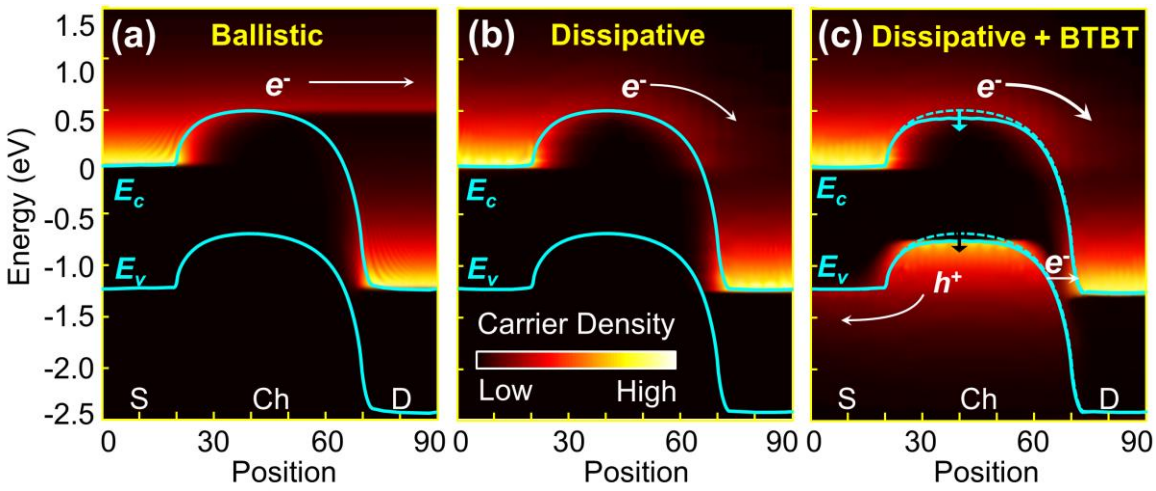


Figure 201: Comparison of the new methodology with old methods.

Energy resolved electron density plots at V_G = -0.6 V; V_D = 1.2 V: E_g = 1.2 eV. (a) Ballistic transport – electron wave propagates without energy relaxation (flat color contour in the channel). (b) Dissipative transport – carriers keep relaxing energy due to scatterings (non-uniform color contour in channel). Single-band model without BTBT capability is shown, where only electrons are considered. Since 2D FETs are far from ballistic, (b) can give more accurate electron current compared to (a). (c) Dissipative transport based on two-band model with BTBT capability. The difference in essential physics can be observed in (c) compared to (a, b), where holes are generated by BTBT and pile up in the channel regions, changing the channel potential (from dashed to solid curves) and thus inducing more drain leakage.

The scattering strength is obtained from the low-field mobility used as input, and described by the probe self-energy Σ_P, included in the self-energy matrix Σ in the NEGF formula $G(E) = [\, E - H - \Sigma \,]^{-1}$, where E is the energy and H is the 2-band Hamiltonian. Subsequently charge distribution and current are solved by NEGF and electrostatics is solved by Poisson's equation in a self-consistent iteration loop. A comparison of this "*BTBT*

+ *dissipative*" method with the old "*BTBT only*" or "*dissipative only*" methods is given in **Figure 201**. The differences in essential physics can be clearly observed, indicating the necessity of the new simulation scheme for GIDL.

C. Dependence on Material Properties

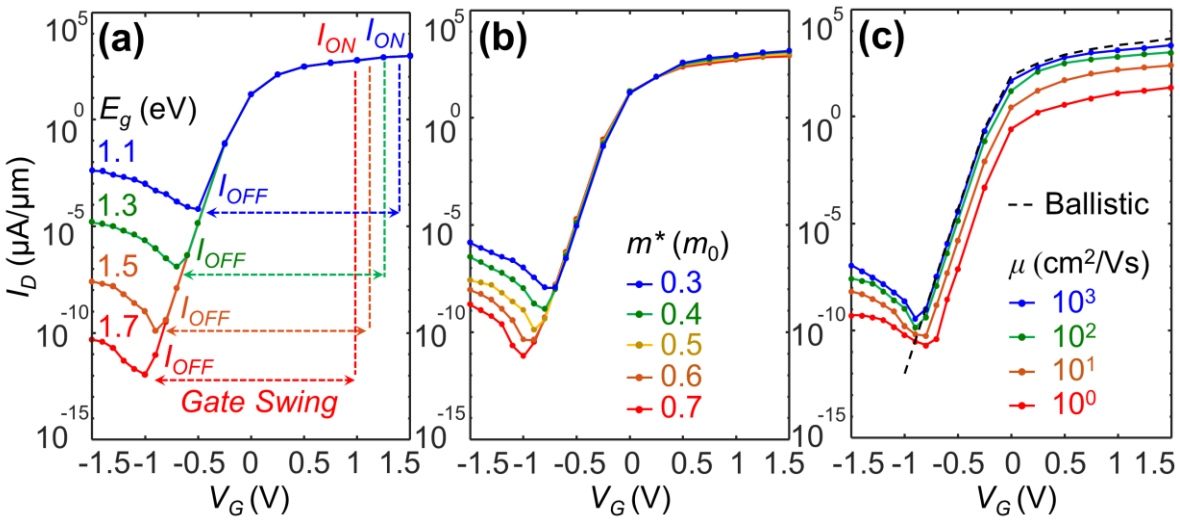


Figure 202: Dependency of I_D-V_G on material properties.

I_D-V_G curves for varying (a) band gap (E_g); (b) effective mass (m^*); (c) mobility (μ). It can be observed that the minimum OFF current (I_{OFF}) has strong dependency on E_g and intermediate dependency on m^* and μ, while the dependencies of ON current (I_{ON}) are negligible on E_g, weak on m^* but strong on μ. The default E_g, m^* (both electron and hole), and μ (both electron and hole) values are 1.5 eV, 0.5 m_0 and 100 cm²/Vs for this chapter, if not mentioned otherwise.

2D materials have wide varieties of basic properties such as band gap (E_g), effective mass (m^*) and mobility (μ), which affect their *I*-*V* curves in different ways, as shown in

Figure 202.

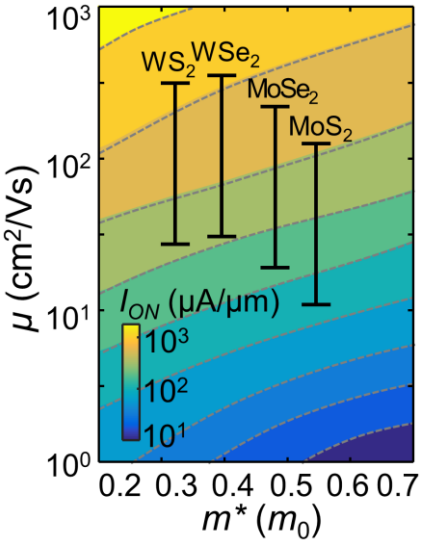


Figure 203: Contour showing I_{ON} dependency on m^* and μ.

I_{ON} is extracted as illustrated in Figure 202a, with a gate swing of 2 V. Some representative 2D TMD semiconductors are marked on the plot. The error bars indicate variation ranges of mobilities (including both experimentally demonstrated and theoretically predicted values).

Moreover, even for a certain 2D material, the values of its properties (especially μ) are reported quite differently by different groups. Hence, instead of simulating and comparing each known material, we conducted I_D-V_G simulations by sweeping every possible combination of E_g, m^* and μ in the ranges of interest (1.1 – 1.9 eV, 0.2 – 0.7 m_0, and 1 – 1000 cm^2/Vs, respectively). First, 216 (9 E_g's × 6 m^*'s × 4 μ's) I_D-V_G curves (5400 data points) were generated. Subsequently, based on this mesh, numerical smoothing and interpolation were used to fill the data continuously in the <E_g, m^*, μ> three-dimensional space. Then I_{ON} and I_{OFF} contours are plotted vs. <E_g, m^*, μ>, as shown in **Figure 203** and **Figure 204**, respectively, from which one can look up and predict the performance of most 2D

semiconductors of interest or engineer new ones. It can be observed that I_{OFF} has strong dependency on E_g and intermediate dependency on m^* and μ, while the dependencies of I_{ON} are negligible on E_g, very weak on m^* but strong on μ. Notably, TMD materials such as MoS_2, WS_2, $MoSe_2$, WSe_2, and ReS_2 show reasonably low GIDL below 10^{-10} μA/μm.

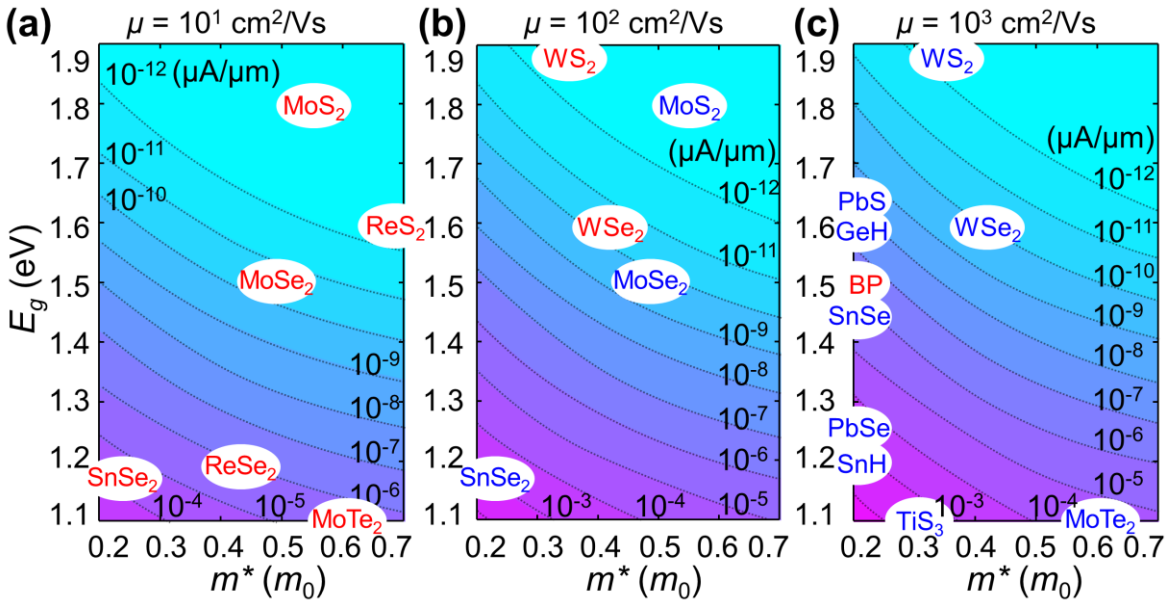


Figure 204: Contours showing I_{OFF} dependency on varied E_g and m^* at different μ.

(a) μ = 10 cm²/Vs; (b) μ = 100 cm²/Vs; and (c) μ = 1000 cm²/Vs. Representative 2D materials are marked on the plots to indicate the corresponding I_{OFF} that can be achieved. "Red" names are based on experimental mobilities while "blue" names are based on theoretically predicted mobilities. It is worth noting that 1L black phosphorus (BP) as well as other group IV-VI 2D compounds are not suitable for low-leakage purpose due to their low m^* and E_g, while some TMD materials such as MoS_2, WS_2, $MoSe_2$, WSe_2, and ReS_2 show relatively low I_{OFF}.

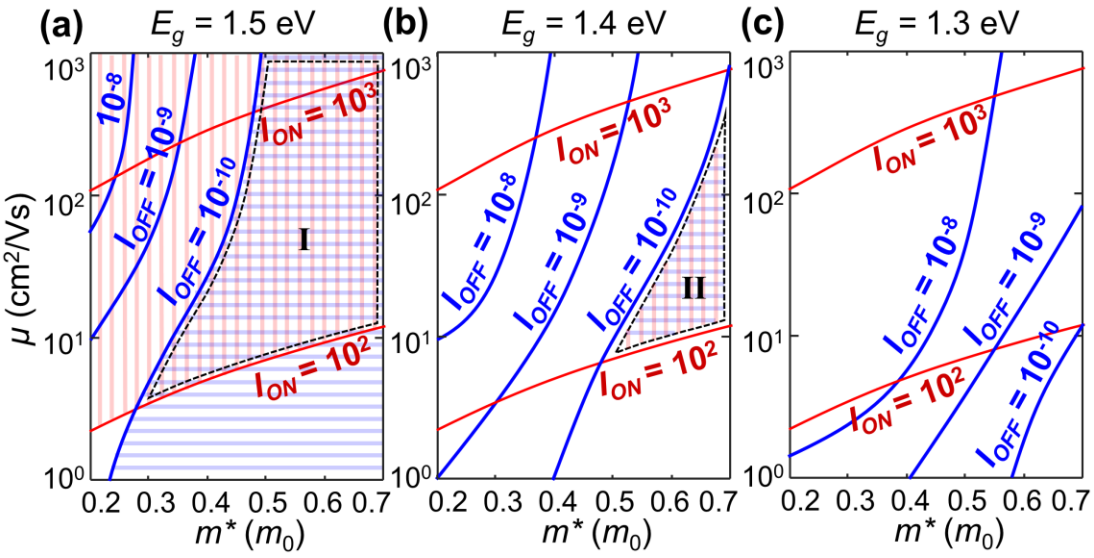


Figure 205: Limitations of m^* and μ for different device performance metrics.

Limitations of m^* and μ for device performance metrics of $I_{ON} \geq 10^2$ and 10^3 μA/μm and $I_{OFF} \leq 10^{-8}$, 10^{-9} and 10^{-10} μA/μm, at E_g's of (a) 1.5, (b) 1.4 and (c) 1.3 eV. For example, as indicated by the red patterned region in (a), the metric of $I_{ON} \geq 10^2$ needs m^* and μ to be bounded in the region above the red curve; while as indicated by the blue patterned region, $I_{OFF} \leq 10^{-10}$ bounds m^* and μ in the region to the right of the blue curve. Hence, *Region I* (crossed pattern) in (a) represents the requirements of m^* and μ, for a 2D material with E_g = 1.5 eV under the metrics of $I_{ON} \geq 10^2$ μA/μm and $I_{OFF} \leq 10^{-10}$ μA/μm; while *Region II* in (b) represents the requirement region for a 2D material with E_g = 1.4 eV under the same metrics, from which it can be observed that the extra 0.1-eV E_g in (a) can induce much relieved requirements on m^* and μ. While higher m^* can relieve the need of high E_g, but intensifies the need of high μ, due to I_{ON} requirement. Hence, relatively large E_g (1.6 – 1.9 eV) and intermediate m^* (0.3 – 0.6 m_0) is the most suitable combination, where TMDs such as MoS_2, WS_2 and WSe_2, have the most potential to deliver ultra-low GIDL under 10^{-10} μA/μm together with ON-OFF ratios around 10^{12}.

Using the database above, benchmarking of 2D materials based on both I_{ON} and I_{OFF} metrics is performed. Two I_{ON} metrics (10^3 and 10^2 μA/μm) and three I_{OFF} metrics (10^{-8}, 10^{-9} and 10^{-10} μA/μm) are used as examples. These current limitations clearly bound $<E_g, m^*, \mu>$ into different regions (**Figure 205**) and it can be observed that the parameters of MoS_2, WS_2 and WSe_2 (E_g ~ 1.6 – 1.9 eV, m^* ~ 0.3 – 0.6 m_0, μ ~ 10 – 1000 cm^2/Vs) are the most likely to deliver those metrics. Given the relatively good research maturity of these three TMDs among all the 2D semiconductors, they can be very promising for access device applications with ultra-low GIDL under 10^{-10} μA/μm and ON-OFF ratio higher than 10^{12}.

D. Implications for Memory Access Device Design

1. Dependence on Device Geometry and Bias

GIDL is also determined by geometry and applied bias of the devices, which affect the electric field at the drain-channel junction (ε_{DC}), thus altering the BTBT probability. As examples, I_D-V_G curves for varying gate underlap, S/D doping density ($N_{S/D}$), and drain bias are shown in **Figure 206**. Overall, inducing gate underlap or reducing doping/bias can further lower GIDL by lowering the ε_{DC}, which can further relieve the requirements on material properties and make TMDs such as MoS_2, WS_2 and WSe_2 more robust for low-leakage applications. Sorely scaling channel length has little effect on ε_{DC} or GIDL, but significantly increases subthreshold leakage (sub-V_T) and makes it dominant over GIDL. However, the use of lower EOT, dual/tri-gate or halo implantation in order to overcome sub-V_T can increase GIDL due to stronger ε_{DC}. Increasing number of 2D layers can improve μ and thus I_{ON}, however, E_g drops simultaneously, which increases GIDL.

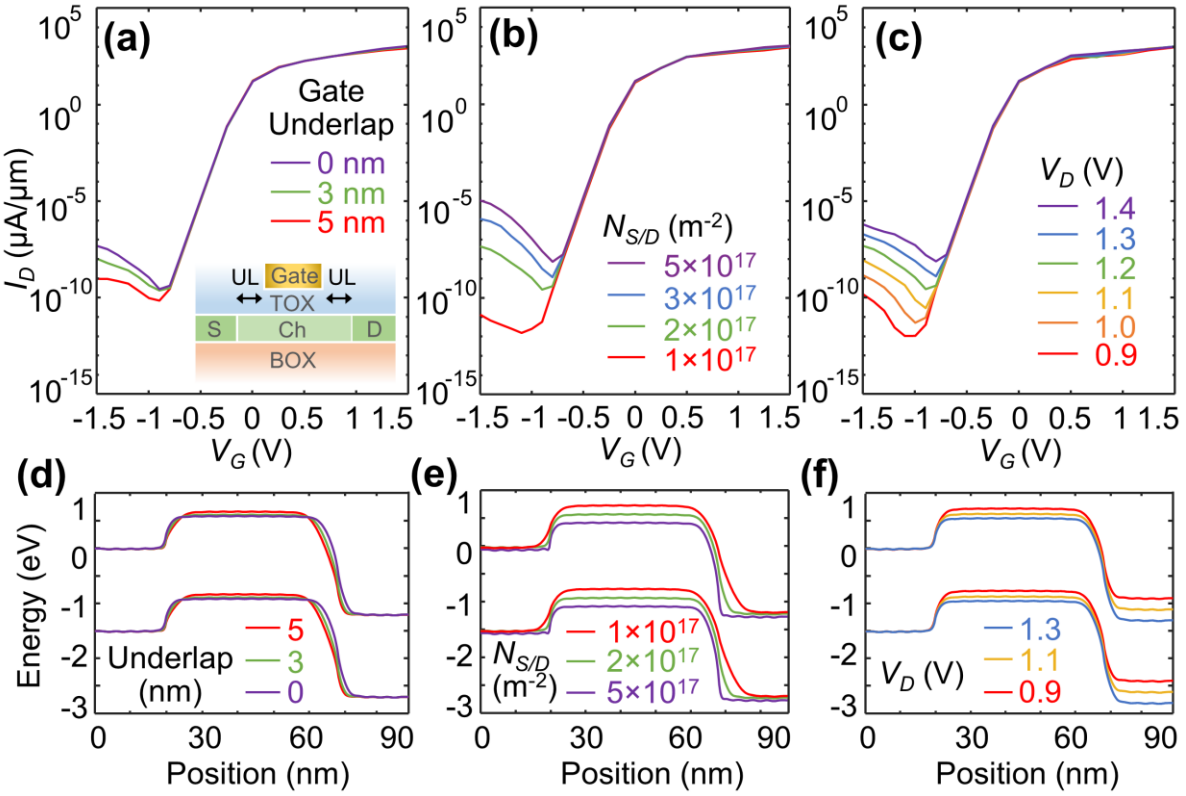


Figure 206: I_D-V_G curves for varying gate underlap, doping and bias.

(a) gate underlap (UL); (b) S/D doping density ($N_{S/D}$); and (c) drain bias (V_D). (d-f) the band diagrams at V_G = -1.5 V, corresponding to (a-c). By optimizing the device geometry, doping and bias, further lowering of GIDL can be achieved, which can further relieve the requirements on material properties.

2. Implications for Schottky-Barrier FETs

Since efficient, precise and stable doping of 2D materials is still challenging, for experimental demonstrations, the undoped junctionless Schottky-Barrier (SB) FET configuration is usually employed instead of the conventional MOSFET structure with highly doped source and drain. Hence, we also extend our study to 2D SBFETs. For

SBFETs, usually one uses ambipolarity rather than GIDL as the description of I_{OFF}, which arises from field emission as well as BTBT across the drain side p-type SB when gate is negatively biased, as shown in **Figure 207a**. It is clear that such leakage is much higher than GIDL in 2D MOSFETs. However, decreasing the SB height can help reduce the leakage, as shown by the I_D-V_G curves in **Figure 207b**.

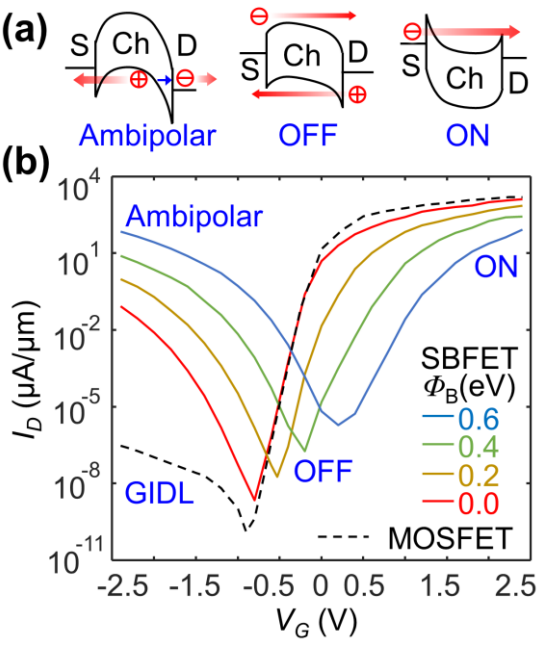


Figure 207: Implications of GIDL on Schottky-barrier FETs.

(a) Band diagram illustrations of 2D Schottky-barrier (SB) FETs at ambipolar, OFF and ON regions. (b) I_D-V_G curves of different SB height (Φ_B). Instead of GIDL, SBFETs exhibit strong am-bipolarity due to the tunneling across the drain side SB.

3. Implications for Tunnel FETs

Finally, in tunnel FETs (TFETs), a transistor architecture which can achieve subthermionic *SS* and low I_{OFF} **[45]**, the GIDL is also larger compared to MOSFETs, since

in TFETs, all the holes generated by BTBT can be drawn by the source, as illustrated in **Figure 208a**. For example, lateral 2D TFETs (P^+-i-N^+ doping profile) **[48]** are compared with 2D MOSFET (N^+-i-N^+ doping profile) (**Figure 208b**). It is suggested that the TFETs should not be overdriven into GIDL condition and S/D doping concentration should be optimized. In comparison, the vertical 2D TFET **[9]** with relatively weak electric field at the drain-channel junction can likely eliminate GIDL.

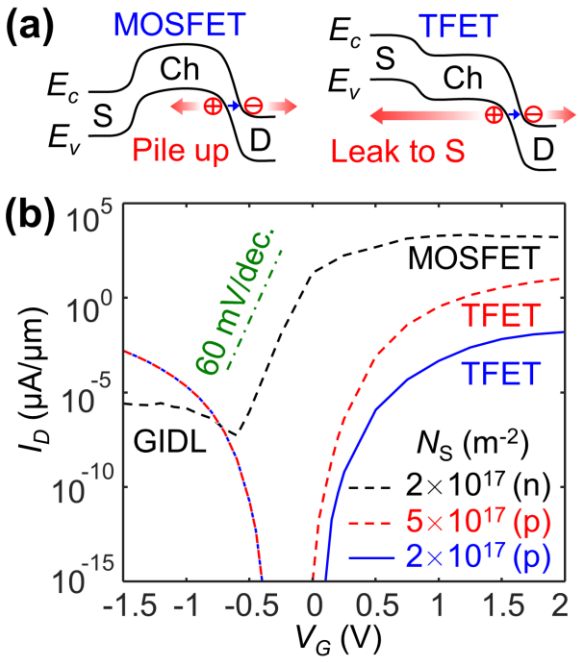


Figure 208: Implications of GIDL on Tunnel FETs.

(a) Band diagram illustrations of MOSFET and tunnel FETs (TFETs) with GIDL. (b) I_D-V_G curves of 2D MOSFET and TFETs, all with an EOT of 1 nm. TFET exhibits higher GIDL since the holes generated by BTBT can be all drawn by the source.

E. Chapter Summary

GIDL in 2D based FETs is comprehensively studied by a novel self-consistent quantum

transport simulator, which can treat both BTBT and various scattering mechanisms. It is found that compared to silicon, TMD semiconductors with relatively large E_g (1.6 – 1.9 eV) and intermediate m^* (0.3 – 0.6 m_0), such as MoS_2, WS_2 and WSe_2, have superior potential to deliver ultra-low GIDL under 10^{-10} μA/μm and ON-OFF ratio higher than 10^{12}. This work provides foundational support to rigorously evaluate the performance and scalability of emerging 2D FETs for their low leakage applications, particularly as access devices in memory technologies.

VIII. Conclusions and Future Work

A. Conclusions on Previous Research

In this dissertation, detailed analysis of the opportunities and challenges for 2D electronic materials are carried out and solutions to address the challenges are proposed and demonstrated. It is also illustrated in this dissertation, that the novel approaches proposed here, can be leveraged to demonstrate completely different device technologies.

First, in-depth physical understanding of the metal contacts to 2D materials is provided. The first detailed methodology for the accurate evaluation of metal contacts to 2D layered materials is presented. Approaches such as interface hybridization and seamless contacts are demonstrated for reducing contact resistance and improving the performance of the transistors based on 2D semiconductors.

Then more interface issues with 2D materials are studied, such as 2D materials' interfaces with dielectrics, substrate and other bulk semiconductors, as well as grain boundaries inside 2D itself. Interface engineering is also explored for steep transistors which are relatively less disruptive compared to present CMOS technology.

In order to realize many electronic devices based on 2D materials, an important process – doping is also investigated and critical strategies are demonstrated for fabrication of various devices, such as transistors interconnects, inductors and electrocatalyst devices. Based on the intercalation doping method the first demonstration of on-chip inductors based on intercalated-graphene, with extraordinary benefits compared to conventional counterparts, is presented.

Finally, GIDL in 2D FETs is evaluated for the first time, using a novel quantum transport methodology. It is shown that certain 2D semiconductors can greatly reduce GIDL.

Material properties and device geometry are also discussed, which provide guidelines for study of low-leakage 2D FETs.

B. Future Work: Integration of 2D with CMOS

As discussed in the previous chapter, one existing challenge for process integration of graphene as well as other 2D materials is how to get rid of the wet transfer process, which is not desirable in state-of-the-art CMOS technologies. Efforts toward low-temperature graphene film growth on dielectric surfaces are needed. Recently, some preliminary works on direct graphene growth on dielectric substrates by CVD has been reported **[171]–[174]**. In these processes sacrificial metal catalyst layers are directly prepared on dielectric substrates and are removed after graphene growth by various etching techniques (dissolution by Marble's reagent **[172]**, Cl_2 dry etching **[173]**, etc.), affording graphene directly on the substrate.

For fabrication of GNRs, lithographic patterning (normally using electron beam lithography for high resolution) of graphene **[142]** is the most natural choice (which is categorized as a "top-down" method), although edge roughness remains a challenge. Other synthesis methods include chemical synthesis **[141], [175], [176]**, selective epitaxial growth **[177]**, unzipping of carbon nanotubes **[178], [179]**, etc. (categorized as a "bottom-up" method), in which the controllability of ribbon width, position, edge quality, and yield are still under improvement.

Another challenge is how to form high-quality interfaces between graphene devices and vias. One possible solution is the adoption of carbon-based vias (as illustrated in **Figure 196**), which can form homogeneous junctions with MLG. Research toward such goal include aligned carbon nanotubes perpendicularly contacting with MLG **[409]**, and the graphenic carbon contacts **[410]**.

C. Future All 2D Electronic Systems

Looking ahead, hybrid integration of various 2D semiconductors (with band gap) as active devices, graphene as interconnects, and 2D dielectrics (such as h-BN), forming "all-2D" logic and memory circuits (**Figure 209**) could be a very attractive pathway for realizing ultra-dense, low-power and flexible integrated electronics. In fact, such 2D-hybridization may not necessarily require different starting materials.

By stacking different 2D device and circuit layers, it is possible to fabricate ultimate high-density, ultra-thin and bendable monolithic 3D ICs with multiple logic/analog/memory layers as well as sensors and solar cell layers (**Figure 209**), which employs the atomically-thin, flexible, bio-compatible, and transparent nature of these 2D materials and cannot be achieved using conventional materials.

A completely new generation of ultra-low power, ultra-dense, "wearable", "implantable" and "invisible" electronics can be envisioned, which will usher unprecedented opportunities in electronics innovation during the next few decades.

The holistic study presented in this dissertation, starting from in-depth physical understanding of material and device behavior under stress to fabrication of energy-efficient digital electronics, memory, photovoltaics and communication systems that either exploit the unique stress conditions or are naturally suitable under such conditions, will contribute to the translation to propel 2D materials from the laboratory into technological applications and help to achieve the vision of the transformative technology of all-2D flexible integrated circuits and systems.

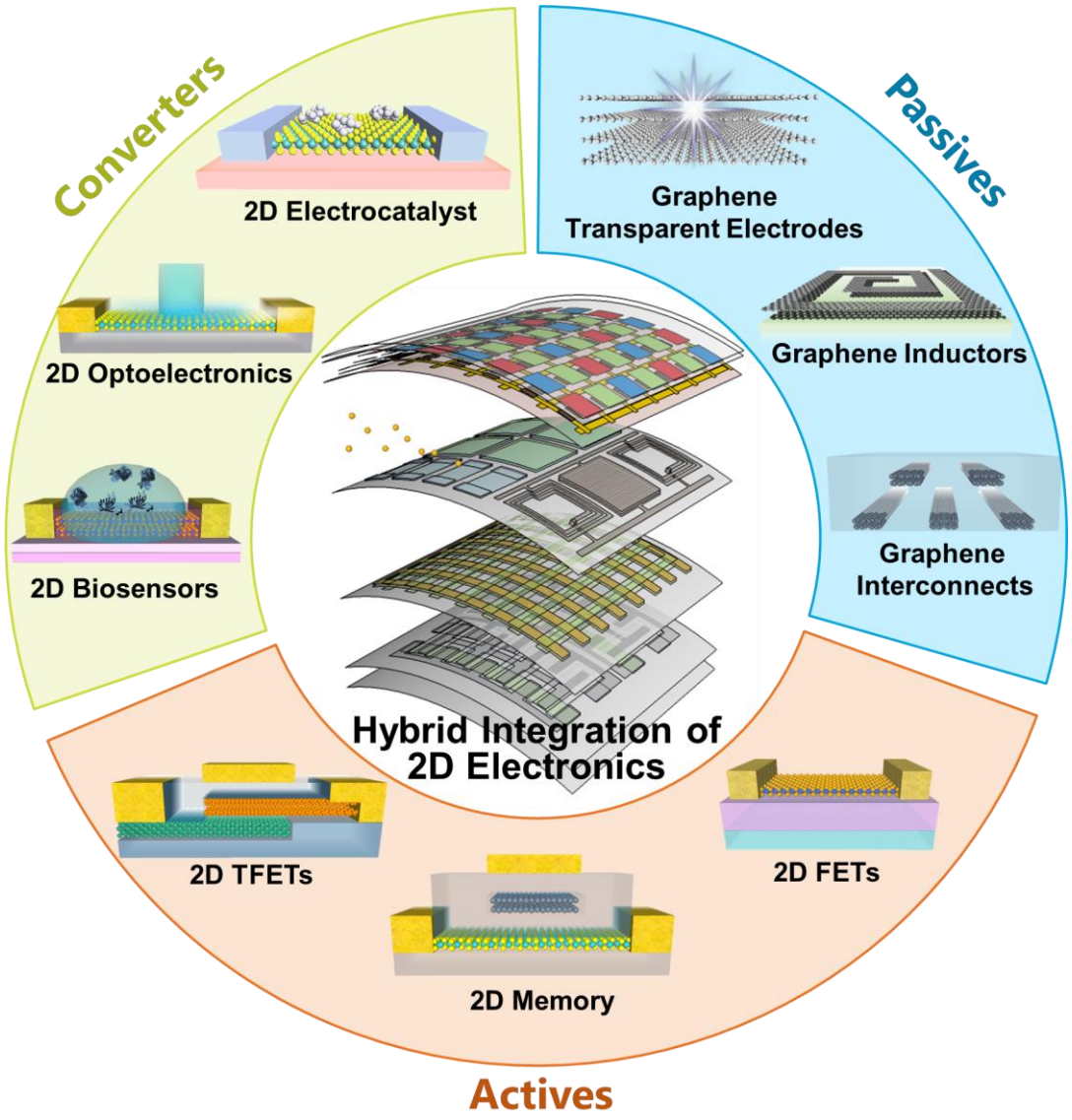


Figure 209: Schematic of an all-2D-material-based 3D-IC.

Active/passive devices as well as energy/signal converters are integrated.

D. Other Thoughts: Environmental Issues

Although graphene and other 2D materials has drawn worldwide researches from various fields including electrical engineering, mechanics and chemistry, very little is known about the fundamental behavior of 2D materials exposed to human environment and human

cells.

For example, a study has shown that graphene, can embed itself in the soil and move through the ground via rain and other water sources, ending up in produce fields. This could affect the growth of produce and, ultimately, the people consuming the produce **[420]**. A series of experiments with human lung, skin and immune cells have shown that graphene can interfere with normal functions of human cells posing serious threats to human and animal health, by piercing through cell membranes with its super sharp and super strong jagged edges **[421]**.

Fortunately, there is still plenty of time to examine and understand the potential harms of 2D materials and find solutions before 2D materials starts to present widely in human life.

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